DEVELOPMENT OF A 1500 VA
LINE-INTERACTIVE UNINTERRUPTIBLE POWER SUPPLY (UPS)

BY

JIBRIN IBRAHIM OKPANACHI

PGS/2000/1463

Being a thesis submitted to the Department of Electrical Engineering, Faculty of Technology, in partial fulfillment of the requirement for the award of Master of Engineering (M.ENG.) in Electrical Engineering of Bayero University, Kano

JULY, 2004

CERTIFICATION

I certify that this project was undertaken solely by me.

J. I. Okpanachi

PGS/2000/1463

APPROVAL

The content of this report are a true reflection of the project undertaken by Jibrin Ibrahim Okpanachi (PGS/2000/1463). It is hereby accepted by the Department of Electrical Engineering, Faculty of Technology, Bayero University, Kano in partial fulfillment of the requirement for the award of Master of Engineering in Electrical Engineering (M.ENG. ELECT.) of Bayero University, Kano.

…………………………… ……………………
Prof. James Katende Date
Project Supervisor

…………………………… ……………………
Alh. S. Sanusi Date
Head of Department

…………………………… ……………………
External Examiner Date

DEDICATION

To the sweet memory of my beloved mother,

Hauwa Ibrahim

To my loving wife

Hauwa Jibrin

and

to my loving daughter

Hauwa (Jnr.) Jibrin

ACKNOWLEDGEMENTS

My profound gratitude goes to the Almighty God, who made this exercise a possibility.

I am sincerely grateful to Prof. James Ketende, for his understanding, criticism and valuable assistance in the execution of this project.

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TABLE OF CONTENTS

CHAPTER ONE:

ABSTRACT

The urgent need for an alternative source of power supply to meet the power requirement of the Electronics/Communications Department of the Nigerian Airspace Management Agency (NAMA), Ilorin Airport, particularly during times of heavy traffic flow, forms the basis for which the development of this cost-effective, reliable and tropicalised uninterruptible Power Supply (UPS) was undertaken.

The developed UPS is required to provide a 1,500VA of an alternating current (a.c) output power at a frequency of 50Hz from a 24V/60Ah direct current (d.c) battery source.

Before the project development commenced, a thorough investigation was carried out on the different UPS topologies currently in use. The line-interactive type UPS topology was found to be the most attractive and the preferred for the Agency’s power supply need.

To realize this, specialized integrated circuits (Ics), power amplifiers, a specially wound inversion transformer and a network of control switches would be utilized. All these basic individual units that constitute the UPS were built into modules after the UPS system had been designed. These modules would be tested individually and wholly (interconnected) as a complete system and then mounted together with transformer in a designed metal casing constructed for the UPS, with input/output sockets, external power control switches and equipment status indicators appropriately provided.

Presented in the thesis is a comprehensive technical review of the available UPS topologies, review of the constituent parts of a UPS, design and constructional details of the developed UPS.

Results of tests performed will be analysed and recommendations for improvement would be given at the end of the report.

CHAPTER ONE

1.1 INTRODUCTION

An Uninterruptible Power Supply (UPS), according to a standard jointly issued by the National Fire Protection Association and the American National Standards Institute (NFPA/ANSI) is defined as “a system consisting of a battery source, a converter, an inverter, and a control equipment designed to provide a clean, conditioned sinusoidal wave form of power for a finite period of time. The UPS usually monitors and tracks voltage and frequency of the normal source. It may be the preferred (on-line operation) or the alternate (standby operation) source of power to the load”. An inverter is basically a device, circuit, or system that delivers alternate current (ac) power when energized from a direct current (dc) power source(2). Stated another way, inversion is the reciprocal function of rectification. Rectifiers change ac into dc, whereas inverters behave in the convase fashion – they turn dc into ac. Inverters appear in myriad applications under other names as choppers, feedback oscillators and relaxation oscillators. An inverter can be an oscillator, and an oscillator can be used as an inverter. General usage used to favour the term “inverter” when the operating frequency is less than about 100KHz, and when the implemented function is to provide ac power for some other circuit or equipment. However, modern inverters are no longer limited in frequency.

A converter on the other hand, is a circuit or system that both receives and provides dc power, in which ac is generated as an intermediate product in the flow of energy. Emphasis is placed on the intermediate product (ac) here as not all circuits that are powered by dc and deliver dc, such as potentiometers, voltage dividers, and attenuators, can be referred to as converters.

In all UPS systems, a comprehensive network of switches/relays, voltage comparators and timing circuits work in tandem to provide switching control function as well as ac line parameter (frequency, voltage, etc) monitoring. The dc power is derived from a battery source in this project. Depending on the type and topology of a particular UPS, the dc power can equally be sourced from the ac line after it has been stepped down, rectified and filtered. This thesis deals with the development of a 1500VA line-interactive uninterruptible power supply (ups).

1.2 MOTIVATION

The motivation for this project derives from the urgent need to meet the power supply requirement of the Electronics/Communications Department of the Nigerian Airspace Management Agency, (NAMA), Ilorin International Airport.

The department is saddled with the responsibility of providing safe operation and maintenance of telecommunications and navigational aids equipment such as HF and VHF radio sets for ground/ground and ground/air communications respectively, telephone/ intercom facilities, Very high Omnidirectional Radio (VOR), Instrument Landing System (ILS) and Distance Measuring Equipment (DME) amongst others, to facilitate free flow of information mainly between pilots (air-borne) and airport (ground base) station, as well as within and between airports.

The effective and continuous usage of the above facilities help to ensure safety of airport operation, enhances safety of the nation's airspace to international standards as well as enhancing national security amongst others. These facilities take in put power from three (3) sources, the public mains supply (NEPA), a standby generator and a standby-on-line hybrid UPS. What then is the motivation for this project?.

i) The public mains supply has become so erractic in nature rendering it grossly unreliable that the NAMA prefers to run her equipment on the standby generator during times of heavy traffic flow.

ii) The standby generator, on the other hand, is not only ageing but the ever increasing high cost of fueling it coupled with the problem of lack of replacement spare parts, has become burdensome to and overbearing on the Agency's lean purse.

iii) The "availability" of the standby on-line UPS that is to supply power in the event of power failure before the generator could be started has also grossly depreciated due to its very high "mean time to repair", caused by lack of spare parts as over seventy (70) percent of its identified faulty units/sub-systems have to be ordered for from outside the country to bring the system back to serviceability status.

With the above myriad of problems, the need for the urgent execution of this project cannot be better justified. Moreover, the poor state of the Nation's Electric Power System calls for urgent measures to produce locally made alternative power supply units for other sensitive loads such as computers systems and life support equipment.

1.3 AIMD AND OBJECTIVES

The main aim of the study is to investigate and analyze the various UPS topologies and to develop a realizable UPS design that would be reliable, cost effective, efficient, maintainable and tropicalised.

The UPS is to be powered from a $24V_{dc}$/60Ah battery source and it is to generate a 220Vac/50Hz with a power rating of 1500VA.

To realize this goal requires vigorous design and assemblage of different electronics components and devices that constitute the UPS system. As a result, the objectives of the study include:

i) Study and analyse the various UPS topologies in the market to identify a suitable one for the department.

ii) Development of an inverter with the desired frequency and voltage rating capable of providing the power requirement.

iii) Development of a ‘window’ comparator to monitor and set allowable limits for the a.c input line, and a feedback control on the ups output voltage.

iv) Development of a switching network of relays and their associated timing and driving circuits to provide the needed control.

v) Design and winding of a suitable transformer for the inversion process.

vi) Coupling of all the developed subsystems and installing them in a suitable enclosure (housing/casing) provided with appropriate connectors/socket for input/output power and system status visual indicators.

1.4 METHODOLOGY

For reasons of fault tracing and maintenance, a modular approach will be adopted. The various units that constitute the system shall as far as possible be separately built on printed circuit boards, tested and then eventually inter-connected as appropriate to give the desired result. For reasons of operational flexibility, reliability, and reproducibility, specialized integrated circuits (Ics) will be used as much as applicable.

The developed UPS will finally be subjected to extensive functional and performance tests to ascertain its efficiency.

1.5 THESIS OUTLINE

This report consists of four chapters including this chapter. Chapter two gives a technical analysis of the different UPS topologies in current use as well as a technical literature review of the basic components/sub-systems that make up a line-interactive UPS system.

Chapter three is concerned with details of circuit approach and system implementation. Constructional details, overall system assemblage, tests and result analysis also form part of this chapter, which ends with the bill of engineering measurements and evaluation for the project undertaken.

Drawn up conclusions, summary and recommendations are presented in the final chapter.

CHAPTER TWO

LITERATURE REVIEW

2.1 INTRODUCTION

Investigation and analysis of the many UPS systems in the market today reveal that there are different types of UPS hybrid topologies that cannot be categorized under the classical standby type UPS and the on-line type UPS. This chapter presents highlights on the different types of UPS topologies with emphasis on their mode of operation. The chapter also gives an over view of all the basic units that constitute the line-interactive UPS that is being developed as presented in this thesis.

2.2 THE CLASSICAL UPS

Classically, UPS systems are intended to improve the quality of ac power in order to provide uninterrupted operation of the ac powered equipment. To accomplish this function, a UPS takes in normal quality utility ac power and provides two enhancements:

i) power quality enhancements

ii) a redundant (back up) power source.

Power quality defects, which may be improved by the UPS include surges, noise, or sags. A UPS system provides redundant power by supplying the load with a primary power source and then providing a back up power source in the case of the failure of the primary source. The block diagram of the general UPS is shown below in figure 2.1.

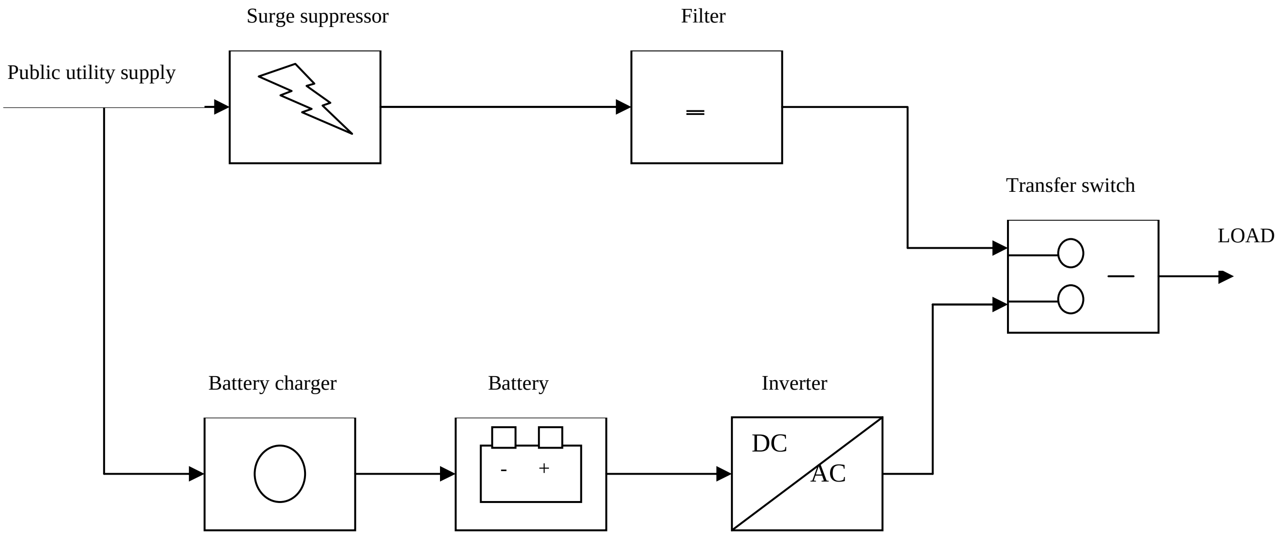


Figure 2.1 The General UPS block representation

2.2.1 Standby And On-Line Ups Systems

The UPS may be operated as either a standby type UPS or an on-line type UPS. The main difference is which power path is chosen to be the primary power path. In figure 2.2(a) and (b) shown below, the solid power path is the primary power path, and the dashed power path is the backup power path.

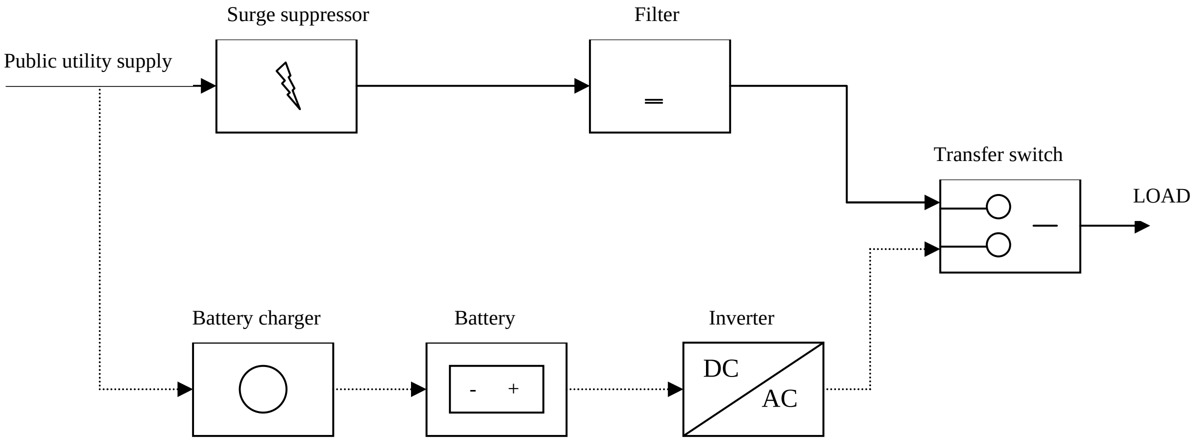


Figure 2.2 (a) Standby mode UPS

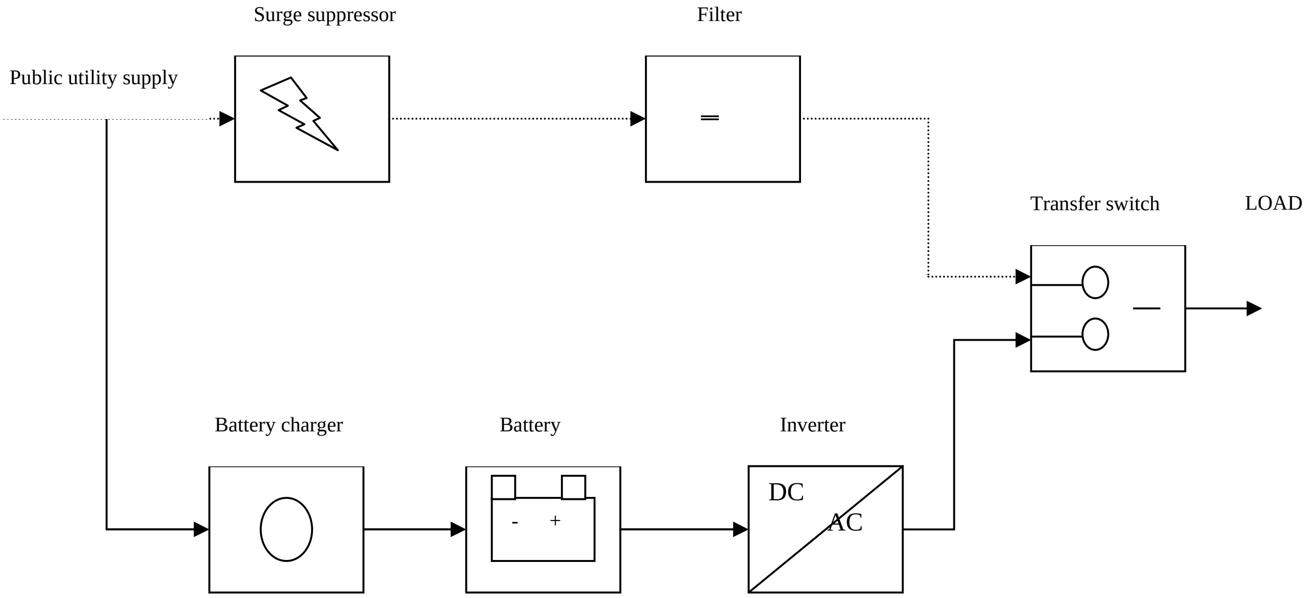


Figure 2.2 (b) on-line mode UPS

For standby UPS operation, the transfer switch is set to choose the filtered ac input as the primary power source, and switches to the battery/inverter as the backup source in case of the failure of the primary source (a.c). In the on-line operation, the transfer switch is set to choose the battery/inverter path as the primary source, and switches to the input a.c as the back up in case of the failure of the primary source (battery/ inverter). This distinction between the online and standby operations is very simple, but it gives rise to some important differences in operation.

2.2.2 Operational Differences Between Standby And On-Line Ups Systems

One interesting difference between standby and on-line operating of the general UPS is the operations during an input ac power failure. In the case of standby UPS operation, the transfer switch must operate to switch over to the battery/inverter backup power source. However, in the case of the on-line operation, failure of the input a.c does not cause activation of the transfer switch. This is so, because, the input a.c is NOT the primary source, but is rather the back up source. Therefore, during an input a.c power failure, on-line operation results in no transfer time.

The on-line mode of operation exhibits a transfer time when the power from the primary battery charger/ batter/inverter power path fails. This can occur when any of the blocks in this power path fails. The power can also drop out briefly, causing a transfer, if the inverter is subjected to sudden changes in the load, or if the inverter experiences an internal control “glitch”. In actual sense, on-line UPS systems do exhibit a transfer line, and in actual installations may transfer as frequently as standby type UPS systems, however, on-line UPS transfers are not related to ac input power failures as they are in a standby UPS.

The size of the battery charger is greatly affected by the choice of standby versus on-line operation of the general UPS. When used in the on-line mode, the battery charger must be large enough to handle all of the output power in order to prevent the battery from discharging.

When used in the standby mode, on the other hand, the battery charger becomes comparatively smaller as it is only needed to supply the small battery recharging power.

The heat generated by the UPS is much larger when the general UPS is operated in the on-line mode. The flow of power through the batter charger and inverter causes a power loss of about 25 to 30 percent. This power loss generates heat, which shortens the lifetime of the electrical/electronics components in the UPS and drastically reduces the life of the battery (the negative effect on battery life is eliminated if the batteries are in a separate compartment/cabinet). When operated in the standby mode, the power loss of the filter and surge suppressor are an insignificant 1 to 2 percent. Over the life time of the UPS, the cost of the extra waster electricity required when the UPS is operated in the on-line mode will be a significant fraction of the original cost of the UPS itself.

UPS systems that exhibit the classical on-line UPS topology include some models from SOLA and TOSHIBA. Units which follow the classical standby approach include the APC Back-ups, Emerson Accupower, and the Sola Sidekick.

2.3 OTHER UPS TOPOLOGIES

Many UPS systems available today are not of the classical standby or on-line type. These UPS systems use a variety of approaches which, as mentioned earlier in the introduction, include:

- i) on-line without by pass
- ii) standby on-line hybrid
- iii) standby-ferro
- iv) line-interactive

2.3.1 The On-Line Without Bypass Topology

In this topology, the general UPS is set up to operate in the on-line mode but the entire back-up power path is absent as shown below in figure 2.3

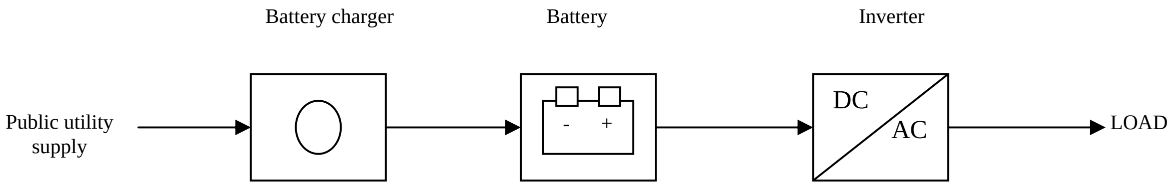


Figure. 2.3: The on-line without bypass type UPS

In this topology, the UPS does not provide a backup power source in case of the failure or glitch of the primary source (inverter). As a result, one important characteristic of a UPS, namely redundancy, is not achieved by this UPS type. This UPS does not exhibit a transfer time during a power failure and is for that reason frequently portrayed as an on-line UPS.

Large UPS systems for microcomputers and mainframes are never of this type, but the lack of the back-up power path (often referred to as a “bypass”) is not frequently recognized in the less experienced pc market place and therefore this type of UPS is sometimes sold. The standby/on-line hybrid design is a derivation of this design.

2.3.2 The Standby On-Line Hybrid Topology

The standby on-line hybrid UPS is a modification of the “on-line without bypass” design. In this design, the battery charger and battery connections are modified, and a standby dc/dc converter is incorporated as shown in figure 2.4 below.

The standby converter from the battery is switched on when an ac power failure is detected, just like in a standby UPS. The battery charger is small, just like in a standby type UPS too.

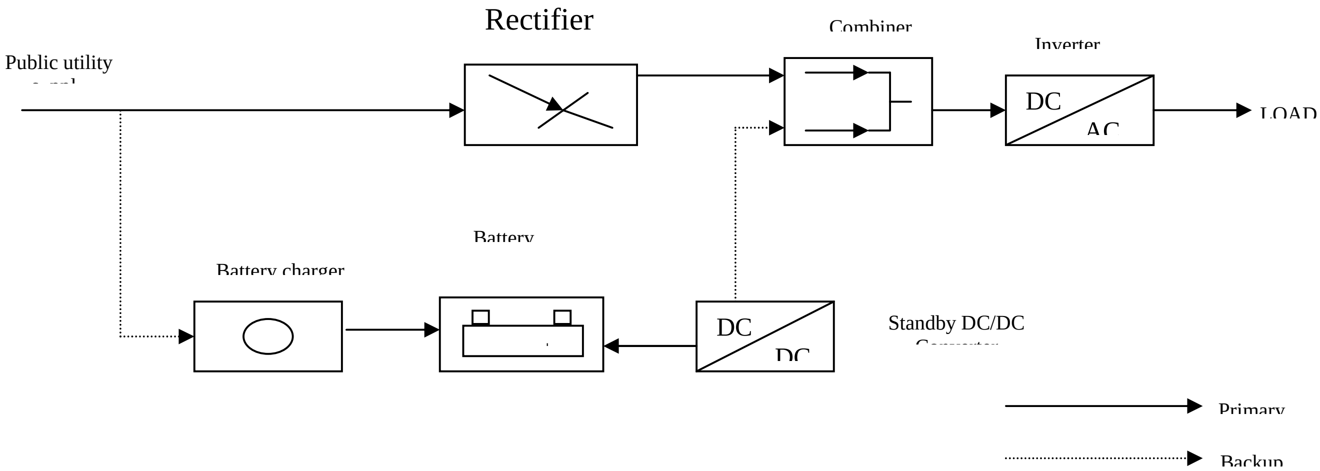


Figure 2.4 The standby on-line hybrid topology

This UPS will exhibit no transfer time during an ac power failure. However, like the “on-line without bypass” type of UPS, this unit has an inverter, which is a possible single point failure for which there is no back-up power path. The most misunderstood part about this topology is the belief that the primary power path is always “on-line” when in fact, the power path from the battery to the output is only half “on-line” (the inverter), while the other half (the dc-dc converter) is operated in the standby mode. Note that in this design, unlike either the classical standby or on-line designs, there is no back-up power path provided in the case of the failure of the primary power path. This topology is used in UPS systems such as the Unison Unipower, and Exide Personal Powerware.

2.3.3 The Standby-Ferro Topology

This design depends on a special transformer that has three windings (power connections). The primary power path is from ac-input, through a transfer switch, through the transformer, and to the output. In the case of power failure, the transfer switch is opened, and the inverter picks up the output load. This is shown in block Figure 2.5 below:

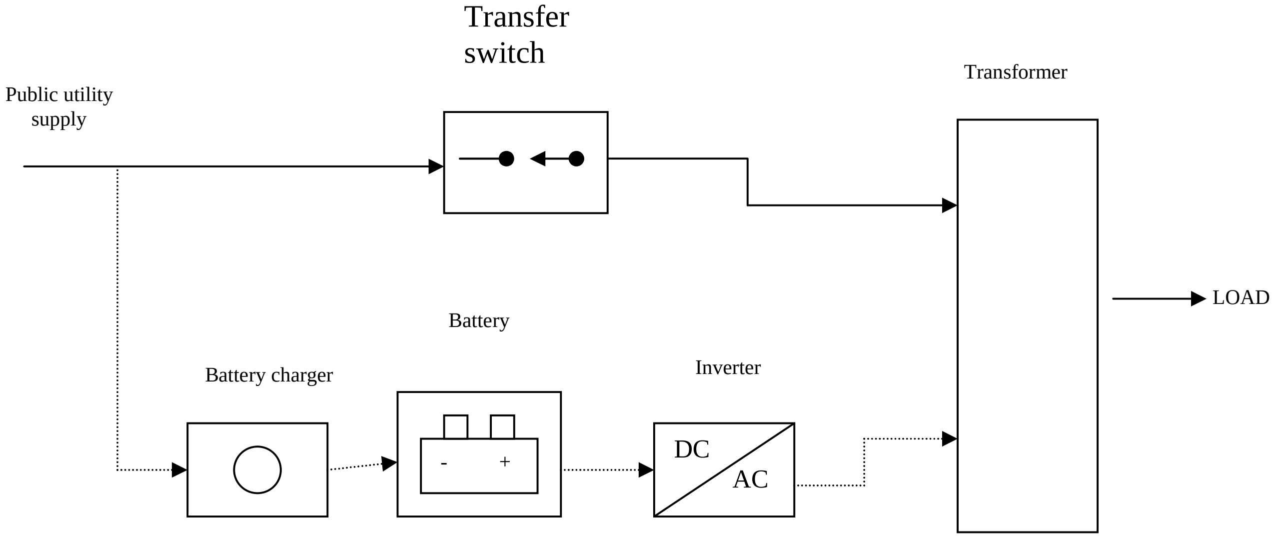


Figure 2.5 The standby-ferro type UPS topology

In this design, the inverter is in the standby mode, and is energized when the input power fails and the transfer switch is opened. The transformer has a special “ferro-resonant” capability, which provides limited regulation and output waveform ‘shaping’. The isolation from ac power transients provided by the ferro transformer is as good or better than any filter available, but the ferro transformer itself creates severe output voltage distortions and transients which can be worse than a poor ac connection. Even though it is inherently a standby UPS, the standby-ferro generates a great deal of heat because the ferro-resonant transformer is inherently inefficient. The best known example of this type of UPS is the BEST Ferrups.

The standby ferro UPS systems are frequently represented as on-line units, even though they have a transfer switch, the inverter operates in the standby mode, and they exhibit a transfer characteristic during ac power failure.

2.3.4 The Line-Literactive Ups Topology

In the line-interactive hybrid topology, the battery-to-ac power converter (inverter) is always connected to the output of the UPS.

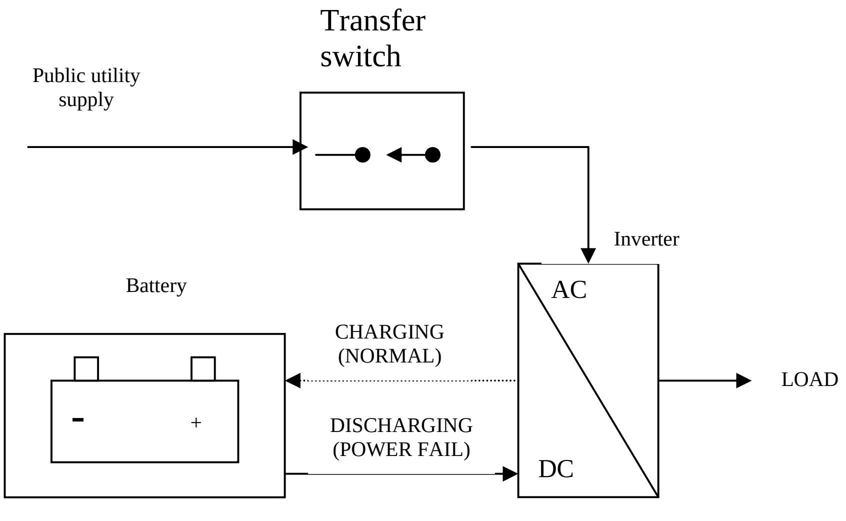


Figure 2.6 The line-interactive UPS

In this topology, battery charging is provided by operating the UPS (inverter) in reverse mode during times when the input ac power is normal, see figure 2.6 above.

When the input power fails, the transfer switch opens and the power flow is from battery to the UPS output. The fact that the inverter is always connected to the output provides additional filtering and reduced switching transients when compared with the other standby type UPS. The inverter also provides regulation, operating to correct brownout conditions, which would otherwise force the UPS to switch to the battery operation. This allows the UPS to operate at sites with very hostile and poor power supply line. This topology allows the design of an inverter in such a way that its failure will still permit power flow from the ac input to the output, which eliminates the potential of single point failure and effectively provides for two independent power paths.

This topology is inherently very efficient which leads to high reliability while at the same time providing superior power protection. Amongst the UPS system using this topology are the American Power Conversion (APC) Smart-UPS and the BEST Fortress UPS.

Evidently, it could be seen from the above that this topology presents the most attractive features and hence its choice for this project.

2.4 THE INPUT VOLTAGE REGULATOR

Power supply is an essential provision needed for any electronic device to function properly. It is desirable that this power supply output voltage remains constant regardless of load current variations or input voltage variations. An electronic control circuit, called a regulator is used to obtain a nearly constant dc output voltage even when there are variations in load or input voltage.

There are linear and switching type regulations that are available in integrated circuit form. In linear regulators, the active component (transistor) operates somewhere between saturation and cut-off and hence it is always ON and dissipates power with efficiency ranging from 50% and below. In the switching type regulator, the transistor operates like a switch. It is either saturated ON or cut-off providing power efficiently from 90% and above.

Due to low cost fabrication technique, there are many integrated circuit regulators available that can be employed for non-critical applications. These include fairly simple, fixed-voltage types and adjustable voltage types.

The simplest of the fixed-voltage type is the three-terminal type. It has only three connections – input, output, and ground, and is factory trimmed to provide fixed output. Typical of this type is the 78xx series. The voltage output is specified by the last two digits of the part number and can be any of the followings: 05, 06, 08, 10, 12, 15, 18 or 24. Typical usage of the +12volt regulator is as shown below in figure 2.7.

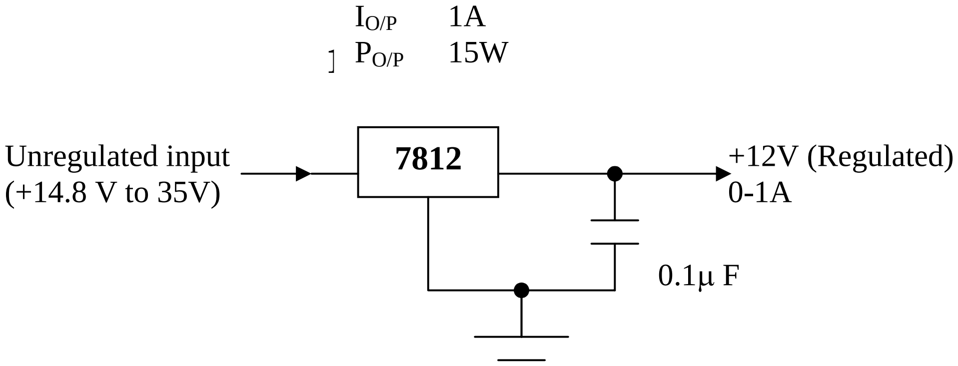


Figure 2.7 The 7812 Voltage regulator.

The output capacitor across the output improves transients response and keeps the impedance low at high frequencies and an input capacitor of at least 0.33μF needed if the regulator is located a considerable distance from the source. They are easy to use and have a number of unique built in features such as current limiting, self-protection against over temperature, remote control operations over a wide range of input voltages and foldback current limiting facility

2.5 UPS SYSTEM WITH SQUARE-WAVE OUTPUT VOLTAGE

AC power supplied by the local electric company is delivered in the form of a sine wave voltage which exhibits a nominal RMS value and 40% higher peak value.

The difference between RMS and peak values of the nominal public mains supply is as shown below in figure 2.4

Peak value = 311V

RMS value = 220V

Ideal AC Sine wave

Figure 2.8 Ideal ac sine wave voltages

The RMS value (a kind of average value) determines the brightness of light bulbs and affects transformers while the higher peak value is used by computers and some communications equipment. The design of a UPS system must take into account the fact that the equipment to be protected will contain a mixture of RMS and peak sensitive loads.

Some UPS systems provide a square wave of voltage to the protected load. This type of wave form cannot meet the requirement of simultaneously supplying the correct RMS and peak voltages to a computer.

It is the nature of square wave voltages that they have peak and RMS values which are equal to each other as shown in figure 2.9 below. The fact that the RMS and peak values are equal means that square wave voltages cannot simultaneously satisfy the differing peak and RMS voltage requirement of typical loads.

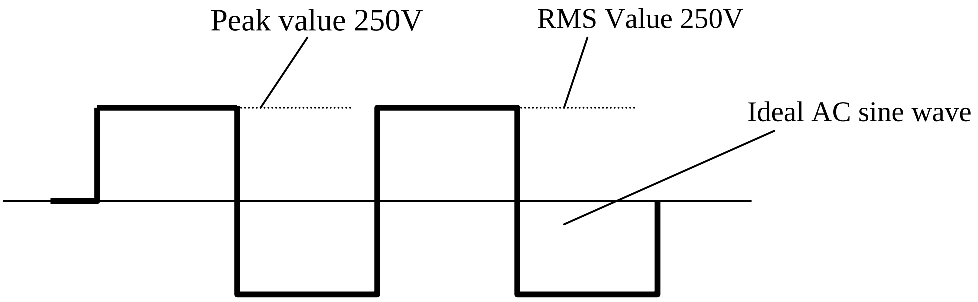


Figure 2.9 Square wave ac voltage

A typical square wave UPS design generates a nominal output voltage of 250volts in an attempt to “split the difference” between 220v RMS and the 311 volts peak value. A design of this type will severely over stress some loads while “starving” others.

The RMS/peak value of a square wave is strongly influenced by the amount of energy remaining in the UPS battery and the size of the UPS load. This means that the voltage provided by a square wave UPS is unregulated and will undergo dramatic swings in voltage of up to 40% during normal operating conditions.

This situation is not acceptable in a UPS application because maintaining a regulated voltage at the input to the load is an important function of any UPS system.

Another waveform which is used for the output voltage of a UPS is called a stepped approximation to a sinewave. In this case, a stepped waveform which has peak and RMS voltages equivalent to a sine wave is produced. This is illustrated in figure 2.10 below:

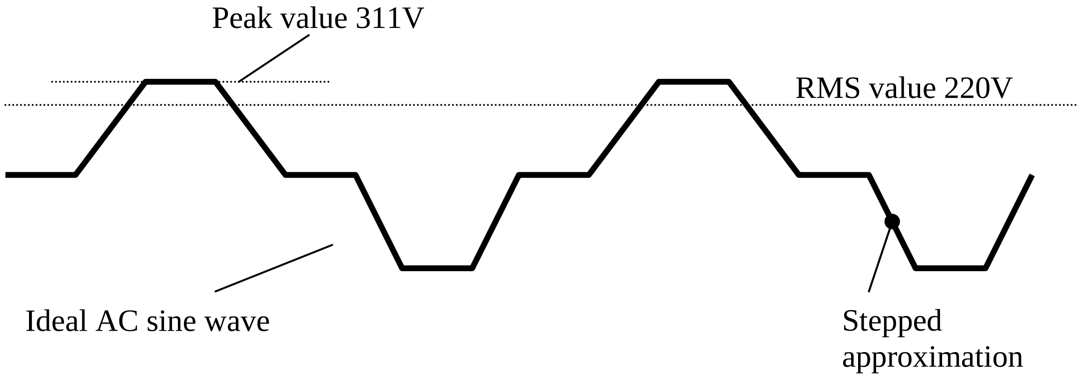


Figure 2.10 Stepped approximation to a sinewave

Another desirable feature of this waveform is that the third harmonic distortion is inherently very low. The output voltage of this project is of the stepped approximation to sine wave a desirable feature of the dedicated pulse width modulator IC (SG3524) used to control the UPS output, and this makes it possible to satisfy both RMS and Peak voltage requirements of different loads.

2.6 CONTROL OF INVERTERS/CONVERTERS WITH SPECIAL IC MODULES

Inverters and converters are often parts of larger overall systems, such as power supplies regulators, motor drives, etc. In such applications, motor drives, etc. In such applications, their outputs are subject to control. The control function may be manual or automatic. One of the most difficult design tasks has been the implementation of low-level and logic circuitry for achieving this control. All manner of problems beset the designer when such control circuitry is made from discrete components.

Moreover, the complexity and resultant cost of such control circuitry often tends to be considerable. In order to obtain reliability, reproducibility, reasonable packaging volume and operational flexibility, it has often been necessary to be reconciled to less than-desired overall performance. It is desirable for the control circuitry to provide such features as soft starting, over load protection, pulse-width modulation, and variable dead time as far as driven inverters are concerned.

The full potential of modern transistors, diodes, transformers and capacitors cannot be realized in the face of such common control malfunctions as jilter, lack of dead time, in unsymmetrical duty cycle, and limited or absent pulse-width modulation capability. These problems can be overcome through the use of special Ics for the control of inverters and converters.

The feature of dead time alone makes these IC modules valuable and a designers delight. This is because one of the difficulties encountered with the otherwise desirable driven inverters is the tendency toward common mode conduction. This arise from the long turn-off time of transistors, from jilter in the drive oscillator, and from the effects of reactive loads. A clean solution to this problem is actuation from a stepped-waveform signal such as the one shown below in figure 2.11.

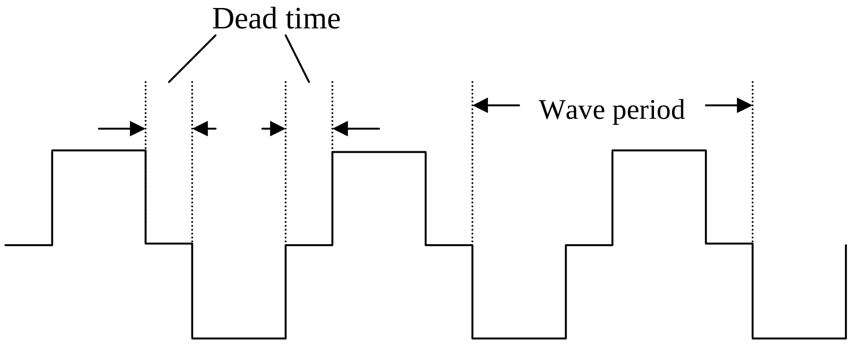


Figure 2.11 Ideal waveform for actuation of driven inverters

These Ics come in 16-pin dual-in-line modules with different pin connections from different manufacturers and under different operating temperature ranges. Examples are the Motorola MC 3420 (0 to + 70^{0}C), MC 3520 (-55 to + 120^{0}C) series, and the Silicon General SG 2524 (0 to + 70^{0}C), SG 1524 (-55 to + 125^{0}C) series.

The SG 3524 used in this project has its pin connection as shown below in figure 2.12

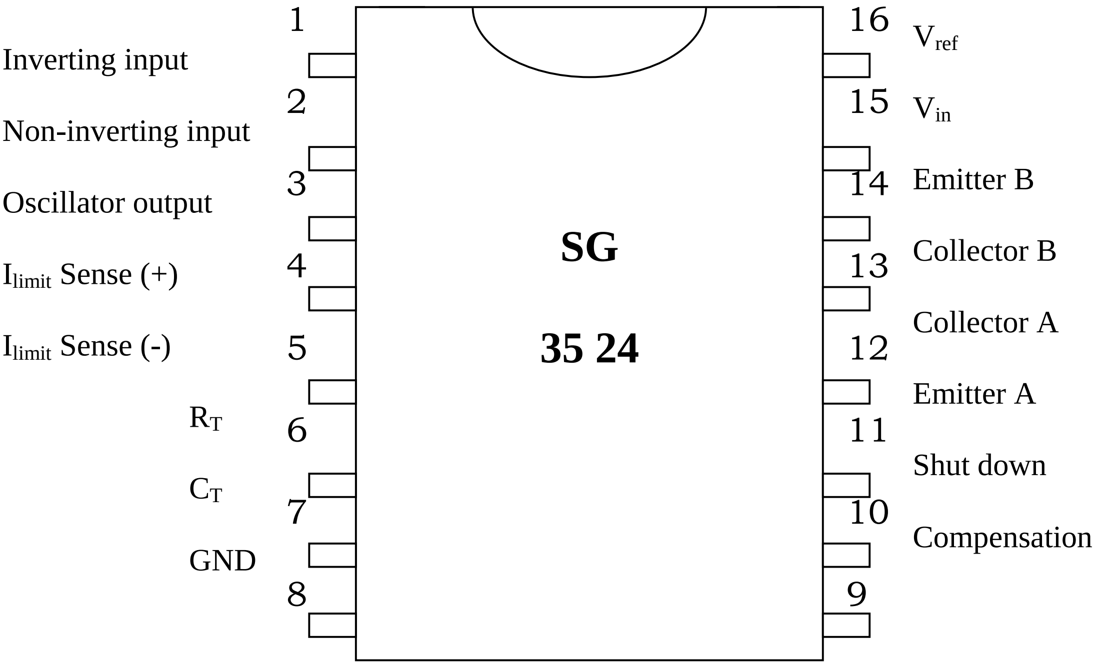


Figure 2.12 SG 3523 Pulse Width Modulator (PWM) Regulator.

With this IC module, the control of frequency is accomplished by means of external timing resistance and capacitance connected to its pin 6 and pin 7 respectively. The oscillator output (pin 3) period is twice that of the output waveforms at pins 12 and 13. A predictable dead band is conveniently obtained by selection of the external timing capacitor. For a given frequency, greater dead band can be achieved by choosing an RC combination in which C has a relatively high value. The connection of a capacitor in the order of 100pF from the oscillator output pin to ground yields even greater dead band if so desired.

To achieve output voltage control, the inverter output is rectified, filtered and attenuated to appropriate level (usually not more than 5V) and then applied to the inverting terminal, Pin 1. By this, the output voltage is sensed and internally compared with a stable reference voltage. The resultant error signal controls the duty cycle of the internal oscillator in such a way as to increase or decrease the output voltage by increasing or decreasing the rectangular pulse duration. This variable pulse duration ensures that both switching transistors that drive the transformer are never switched on simultaneously, thereby eliminating the phenomenon of common-mode conduction.

For the purpose of clarification, the regulatory effect is achievable because the energy stored in the primary winding of the inversion transformer is proportioned to the length of time current passes through it, and the more energy, the higher is the voltage induced in the secondary winding when the switching transistors are alternately off.

The overload protection is offered by the error signal fed back to the compensation pin from the output, as sensed by the internal current limit operational amplifier with its two inputs, Pin 4(+) and pin 5(-) linked to the feedback loop.

With excessive current feed back, the drive signal from the pulse-width modulator is inhibited with the effect that repeated attempts to resume normal operation would fail.

As long as the over load persists, such attempts result is continued shut-off of the drive signal. Normal operation will resume automatically on removal of the over load.

2.7 BUFFER INTERFACE/DRIVER STAGE

Power amplifiers may be classified according to frequency range, the methods of inter-stage coupling used, the bias point at which the active device (transistors or valves) operate, and the aspect of the output signal which is of particular interest, for example, voltage, current or power. Circuits which amplify a wide range of frequencies are known as wideband (or broadband or untuned) amplifiers, and those which are tuned to amplify a narrow range of frequencies are called narrow-band (or tuned) amplifiers.

Methods of coupling amplifier stages modify the performance to some extent. The most common method is a.c (alternating current) coupling, in which low frequency components (including d.c signals) are not transmitted to the following stage. Some others are d.c (direct current) coupled, so that every frequency down to d.c is transmitted to the following stage.

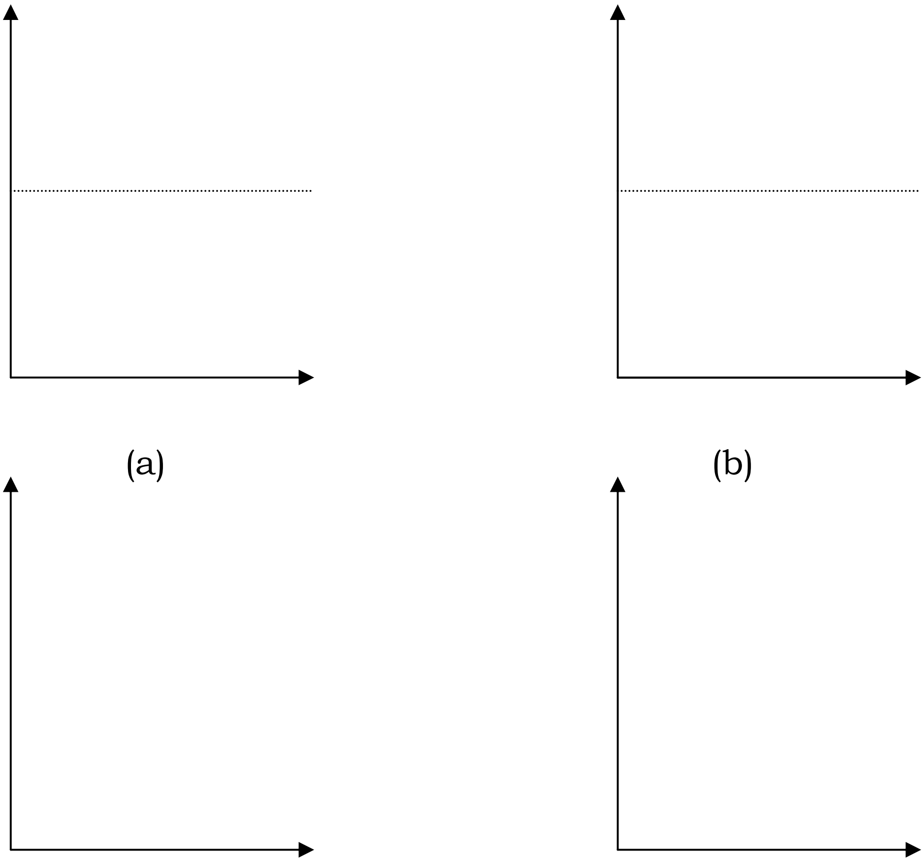
The operating conditions to which the active devices are biased are related to the amplifying function carried out by that stage.

To achieve low distortion amplification of audio-frequency signals, only class-A would seem to apply. In class-A amplifier, current flows in the load during the whole period of the input signal wave.

If, however, one uses complementary-symmetry or a push-pull configuration, class- AB and class – B amplifiers can be obtained to yield linear ear amplification.

In class – AB amplifier, current flows in the load for more than half a cycle, but less than the full cycle of the input signal wave while in class – B amplifier, current flows in the load for half a cycle of the input signal. For the class – C amplifier, current flows in the load for less than half a cycle of the input signal.

There are as shown diagrammatically in figure 2.13 below:



(a) (b) (c) (d)

Figure 2.13: (a) class-A, (b) class-AB, (c) Class-B and (d) class-C amplifiers

The class-C power amplifiers are used extensively at radio frequencies where tuned circuits remove the distortion resulting from the non-linear operation of the circuit.

An amplifier of unity gain is called a buffer because of its isolating properties of high input impedance and low output impedance.

2.7.1 The Complementary Symmetry Push-Pull Class-B Amplifier

A standard class-B push-pull amplifier requires two power transistors of the same type with closely matched parameters. The chief requirement of a complementary amplifier is a pair of closely-matched but oppositely-doped power transistors. The term ‘complementary’ arises from the fact that one transistor is PNP type and the other is of NPN type. They have symmetry in the sense that both are made from the same material and technology and have the same maximum rating.

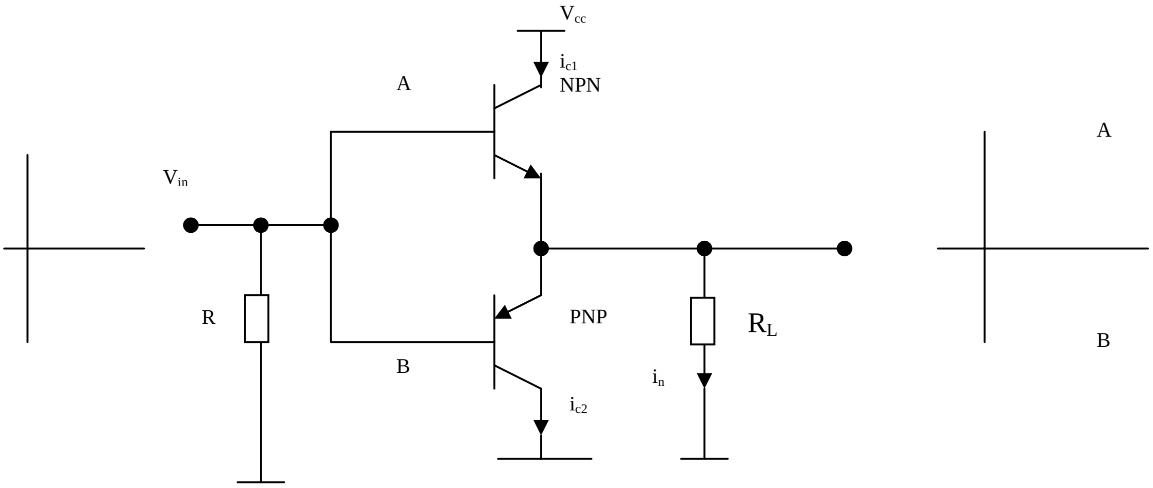


Figure 2.14 Complementary symmetry class-B push-pull amplifier

Diagrammed above in figure 2.14 is a representation of an elementary complementary symmetry class-B push-pull amplifier.

With no input signal, neither transistor conducts and therefore, current through R_L is zero.

When input signal is positive-going, transistor A is biased into conduction whereas B is driven into cut-off. When the signal is negative going, A is turned off while B conducts. The circuit possesses the essential characteristics of an emitter follower, that is, unity voltage gains, no phase inversion and input impedance is much higher than output impedance.

2.7.2 The Bipolar And Mosfet (Bi-Mos) Switch

The concept of using a low voltage fast switching transistor in the emitter of a second high voltage transistor- in a so-called cascode connection – to yield a combined high voltage, high speed switch is not new. This has been achieved in the past using bipolar transistors.

With the availability of power FETS, this cascode technique can be employed, because a high voltage device with FET-like switching performance and relatively low conduction voltage drop can be implemented by combining a high voltage bipolar with a low voltage FET. The best features of each device can be combined to provide operating characteristics that cannot be achieved with either one on its own. This cascode combination of BIpolar transistor and power MOSFET is referred to as a BI-MOS switch. See figure 2.15 below for cascode connection of a MOSFET and a Bipolar.

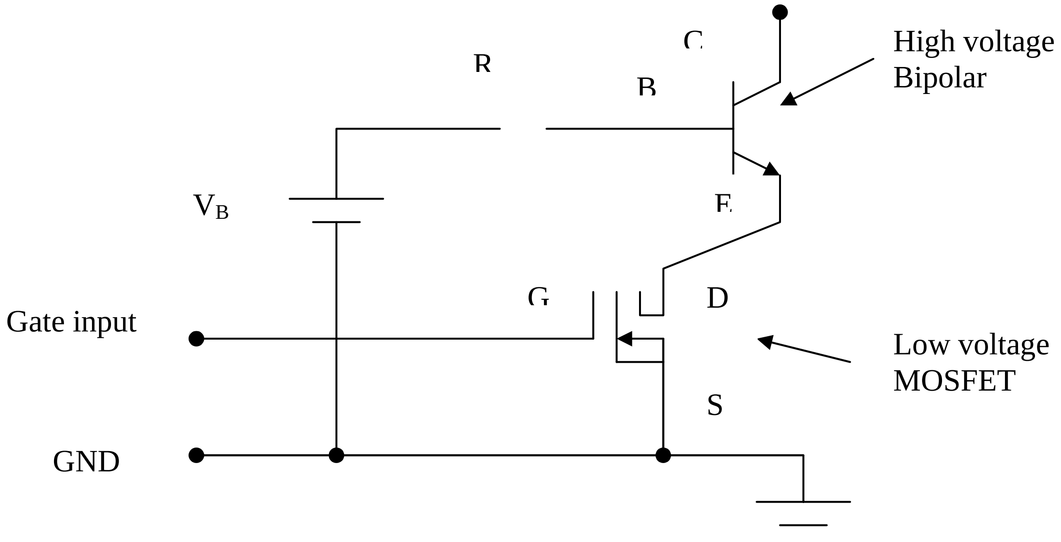


Figure 2.15 Basic BIMOS switch

The circuit operation is such that the device is switched ON and OFF by control of the MOSFET gate. When the FET is ON, the bipolar is ON, since it receives base drive current from the bias supply voltage V_B. When the FET is off, the bipolar is also OFF, since its emitter is open-circuited. The voltage developed a cross the FET when it is OFF is essentially only the bias voltage supply V_B (typically 10-15v).

From the circuit, it would be seen that, the collector-source blocking voltage capability of the combined switch is the relatively high V_{CBO} rating of the bipolar, because of the “common base” configuration.

In addition, the switching speed of the bipolar is much faster than is achieved in the usual common emitter connection. In essence, this is because the forcible opening of the emitter at switch-OFF diverts the collector current in its entirety out of the base.

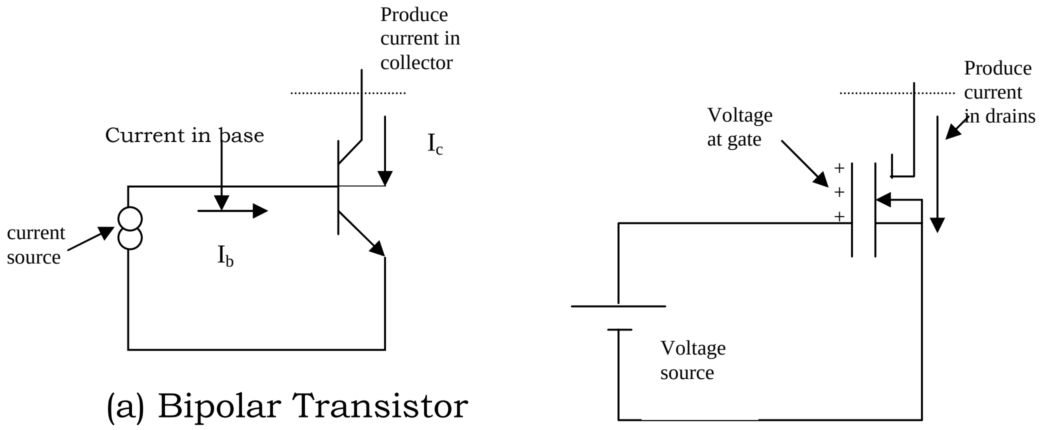
Since the ON or OFF state of the BIMOS Switch is controlled at the gate of the FET, the input impedance is that of the FET; the externally applied drive current is only that needed to charge and discharge the self capacitance of FET. These devices are used in a range of applications such as direct off-line (240v) high frequency (20-250KHz) single ended switching power supplies, and direct off-line (440v/480v, 3-phase) high frequency bridge inverter circuits for motor drives, uninterruptible power supplies, and high power (class-D) switching amplifiers.

Whenever better switching performance is required, interface circuits are normally added to provide fast current sourcing and sin king to the gate capacitances of the FET switch that is to be driven.

2.8 THE FET SWITCH

A common use of FETS, particularly MOSFETS, is as analog switches. Their combination of low ON resistance (all the way to zero volts), extremely high OFF resistance, low leakage currents, and low capacitance, makes them ideal as voltage-controlled switch elements for analog signals(6). An ideal analog, or linear, switch behaves like a perfect mechanical switch: In the ON state, it passes a signal through to a load without attenuation or non-linearity, while in the OFF state it is an open circuit.

FETS are voltage driven as compared to their current driven bipolar counterparts.



(a) Bipolar Transistor

(b) MOSFET

Fig 2.16

(a) Bipolar transistor in current driven (b) FET is voltage driven.

As seen from the above illustration in figure 2.16(a), a current must be applied between the base and emitter terminals to provide a flow of current in the collector. The amount of a drive required to provide a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to provide a flow of current in the collector.

The FET is fundamentally different; it is a voltage-controlled device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain.

The gate is isolated electrically from the source by a layer of silicon dioxide.

Theoretically, therefore, no current flows into the gate when a dc voltage is applied to it – though in practice there will be an extremely small leakage current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalance-voltage.

When a voltage is applied between the gate and source terminals, an electric field is set up within the FET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage. Care must be taken not to exceed the gate-to-source maximum voltage rating of the device used to avoid a loss in performance or outright device failure. It should also be kept in mind that even if the applied gate voltage is kept below the maximum rated gate voltage, the stray capacitance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to destruction of the oxide layer. Over-voltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. As a result, a small resistor or a ferrite bead is usually physically located close to the gate lead to swamp out undesired oscillation and to counter the effect of capacitive loading. The series resistance is a compromise between speed and protection, with values of 100ohms to 10 kilo-ohms being typical.

Another important precaution to be taken while using MOSFETS is to make sure the gates are not left unconnected, because they are more susceptible to damage when floating (there is then no circuit path for static discharge, which otherwise provides a measure of safety). This can happen unexpectedly if the gate is driven from another circuit board. The best practice is to connect a pull-down resistor (say 100KΩ to 1MΩ) from gate to source of any MOSFETs whose gates are driven from an off-card signal source.

2.9 CURRENT RATINGS OF MOSFETS

The major criterion, on which the continuous rating of a MOSFET is based is heat removal. The MOSFET will carry as much current as the cooling system will permit, while keeping peak junction temperature within the rated maximum value. The more efficient the heat dissipator to which the MOSFET is attached, the lower the case temperature will be, the greater the permitted case-to-junction temperature rise, the greater the permitted internal power dissipation, and the greater permissible current. These considerations are exactly the same as those, which apply to other non-gain-limited power semiconductor devices such as rectifiers and thyristors.

The useable current, I_D, for a MOSFET is given by:

$$I_D = \sqrt{\frac{T_{j\max} - T_c}{R_{os(on)} R_{th(Jc)}}} \text{......................} 2.1$$

where $R_{DS(on)}$ is the limiting value of the on-resistance at rated $T_{(Jmax)}$, at the appropriate value of I_D, R_{thjc} is the maximum value of the internal junction-to-case thermal resistance, and T_C is the case temperature.

The all-important factor is, a sufficient heat removal provision must be provided is addition to sufficient gate ‘hard’ drive signal to get the best of MOSFETs when used in switching applications.

2.10 THE TRANSFORMER

A transformer is an electrical device consisting of two closely coupled coils (called primary and secondary) by means of which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It can raise or lower the voltage in a circuit but with a corresponding decrease or increase in current. The physical basis of a transformer is mutual inductance between the coils that are linked by a common magnetic flux. The two inductive coils are electrically separated but magnetically linked through a path of low reluctance.

2.10.1 Principle of Transformer Action

Consider an ideal transformer whose secondary is open and whose primary is connected to a sinusoidal alternating voltage as shown below in figure 2.17

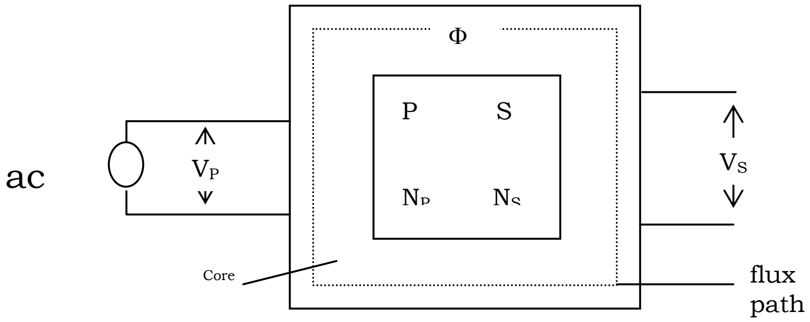


Figure 2.17 Transformer winding.

A laminated iron core carries a primary winding P of N_p turns, and a secondary winding S of N_s turns. The supply (from NEPA) is connected to the primary winding, alternating current flows and produces an alternating magnetic flux in the linking core.

This flux, according to Lenz's law, induces an electromotive force, (emf) to oppose the primary applied voltage V_p and be almost equal to it in a very short time. The two voltages are not exactly equal because of the alternating current - which is called the magnetizing current - flowing through the resistance of the primary winding.

The induced e.m.f. is equal to the number of turns of coil multiplied by the rate of change of flux. If the magnetizing current is assumed very small, then the induced emf equals the applied voltage, hence

$$V_p = KN_p \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.2$$

Where K is the rate of change of flux. As the emf is passed from the primary windings to the secondary, not all the flux links the primary with the secondary. Some gets lost due to the effects of magnetizing currents, magnetic leakage, hysterisis and eddy current losses in the core and the winding coil resistances as is applicable in practical transformers.

If we ignore this loss, or leakage is negligible, the induced emf in the secondary, V_s, is given as

$$V_s = KN_s \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.3$$

As a result, from equations 2.2 and 2.3, we have

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.4$$

This implies that voltage ratio equals turns ratio. The difference between the ideal and the practical transformer therefore lies in the losses.

2.10.2 Transformer Emf Equation

Consider a typical sinusoidal supply voltage from NEPA.

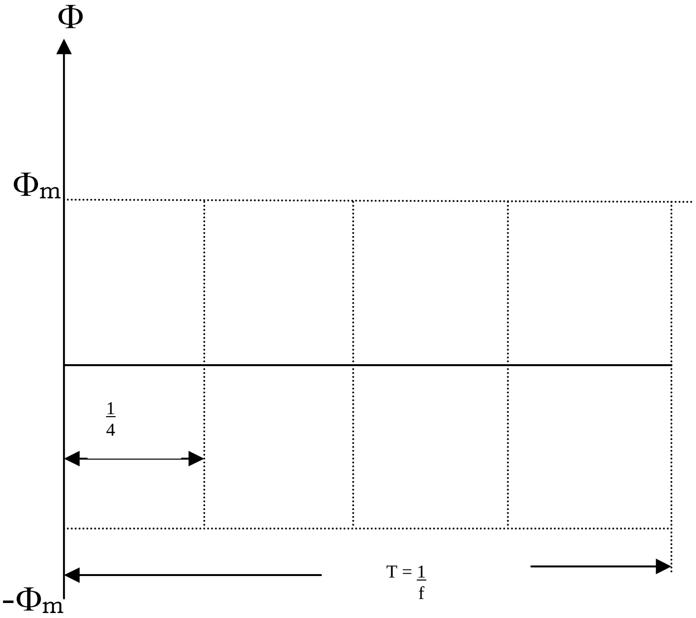


Figure 2.18 Flux variation in the Transformer winding

The flux variation resulting will then be sisusoidal as shown in figure 2.18 above. A change of flux from Φ_m to $-\Phi m$ or 2 Φm takes place is a period T/2, hence the rate of change of flux is:

$$\frac{2\Phi m}{{}^{T}/_{2}} = \frac{4\Phi m}{T} = 4f\Phi m \ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.5$$

From equation 2.2, the average emf induced perturn is 4fN Φ_m.

It is known that for a sinewave, the ratio of rms value to mean value is a constant called form factor with a value of 1.11, and hence

$$V = 4.44N\Phi mf \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.6$$

From equations 2.2 and 2.4 it can be taken that the ratio of the induced emf in the primary to that in the secondary equals to the primary secondary turn ratio and is a constant:

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} = K \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.7$$

This constant is known as the voltage transformation ratio. For K>1, we obtain a step-up transformer and with K<1, we obtain a step-down transformer.

Talking of power in an ideal transformer, input power is equal to output power, that is,

input VA = output VA ,

$$V_p I_p = V_s I_s \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.8$$

From equation 2.8 above, we get that

$$\frac{I_s}{I_p} = \frac{V_p}{V_s} = \frac{1}{k} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2.9$$

Which shows that currents are in the reverse ratio of the (voltage) transformation ratio.

2.11 TRANSIENT SUPPRESSION

Surges or transients are capable of causing severe damage to computer hard wares and other communication equipment connected to supply lines. As a result, surge suppression is an important function of any power protection system. It is to be understood, however, that surges represent a very small fraction of the types of power disturbances that affect computer and other equipment operations. Under voltage conditions, such as dips, sags brownouts and blackouts are responsible for most equipment malfunctions and data loss in computer systems. Ground noise is another factor that poses significant problems for networked or multi-user systems.

Surge suppression or reduction can be accomplished by many different techniques; the “shunt” or “paralled” system and the “isolating” or “series” system.

2.11.1 The Simple “Shunt” System

This is the simplest and most common technique used for surge suppression. The most inexpensive designs of the “Shunt” type use a simple Metal Oxide Varistor (MOV) clamping device. This types of supervisor has a clamping voltage of around 300 to 400 volts which means that 300 to 400 volts is the threshold at which surge suppression begins. With this type of suppressor, surges of less than this threshold value are passed through directly to the user’s equipment.

This design has a characteristic response time called the “clamping response time”. This means that the suppressor takes time to react and may pass through spikes of very short duration without clamping action.

This design is to protect against catastrophic equipment damage and is better suited for use with household appliances than for sensitive loads like computers.

2.11.2 The “Shunt” Design With Filtering

The next level of sophistication combines the shunt type MOV clamping device with electromagnetic interference/radio frequency interference (EMI/RFI) filter.

The EMI/RFI filter is a useful feature but frequently interacts (rings) with the surge clamping device and may cause large transients when excited with a surge test wave form.

Many of the better “Computer-grade” surge suppressors are of this type.

2.11.3 The Silicon Avalanche Diode

This is the type of suppressor where a silicon Avalanche Diode or TRASORB diode is used in place of, or to supplement an MOV. These designs provide a faster response speed than a MOV-only design, and provides marginally better response to repetitive surge bursts. However, the energy rating of even the fastest of these designs is much lower than that of a medium sized MOV.

Some designs employ a “Gas Discharge Tube” clamping device in addition to other features. Gas Discharge Tubes are very slow suppressors to limit the surge if the other “shunt” type elements are overcome.

2.11.4 The “Series” or Isolating Suppressors

The best type of surge suppressor uses a “series” or isolating design. They are more expensive but offer improved performance. In this case, circuit elements are placed between the AC line and the users equipment. The circuit elements are designed so that they will pass the normal 50Hz AC power but have greatly increased electrical resistance at higher frequencies. In this fashion, such components act as “brickwall” to surge instead of mere “diverters”. Available series type elements are not as ideal as desired, usually due to size, cost and heat dissipation limitations, so they are combined with shunt type clamping and filter elements to achieve superior surge reduction performance. The series design, if carefully laid and executed, can result in a zero clamping response time, making the use of TRASORB diode unnecessary. In addition, heroic shunt measures such as the use of Gas Discharge Tubes are not required. The hybrid series/shunt surge suppressor design is used in most power conditioner (sometimes called regulating transformers) and is used in advanced, high performance surge suppressors. This type is used in all APC UPS.

The surge suppressor used in this project is of this type. A line sensing transformer combines with a network of voltage comparators (in the form of a missing pulse detector and a voltage level detector) and some timing/switching circuits to set the surge threshold or transfer voltages levels.

2.12 COMPARATOR WORKING PRINCIPLE

It is quite common to want to know which of two signals is larger, or to know when a given signal exceeds a predetermined value. The most common device to use is the comparator. The simplest form of comparator is a high gain differential amplifier, made either with transistors or with an operational amplifier (op-amp).

Figure 2.19 below shows a symbolic representation of a comparator with signal V_1 applied to the inverting input terminal and signal V_2 to the non-inverting input terminal, and V_0 being the output.

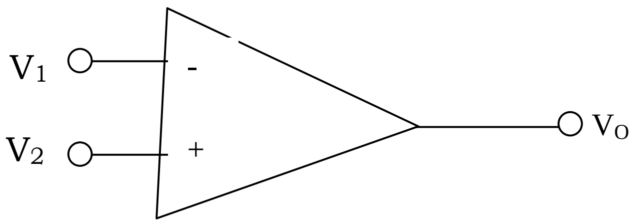


Figure 2.19 comparator symbol

If V_1 and V_2 are equal, then V_0 should be zero. Even if V_1 differs from V_2 by a very small amount V_0 is larger because of amplifier's high gain. Hence, the circuit is able to detect or compare two signal values. They are used in applications such as interface between analog (linear) input signals and the digital world.

A good number of integrated circuit have varying number of these comparators in them. An example is the LM 393, which has two comparators built into it.

2.13 SUMMARY

The different UPS to topologies in addition to the classical on-line and standby mode UPS were discussed with emphasis on their operational differences.

We were also able to discuss UPS systems with square wave outputs voltage with its implications and arrived that a UPS should supply the protected loads with an ideal sinewave or a stepped approximation to a sinewave. Square waveforms can cause loads to malfunction or even become damaged.

Various classes of amplifier circuits were discussed with special highlights on the complementary symmetry push-pull amplifier and a BI-MOS switch that combine to interface between the multi function pulse width modulator IC employed in this project and the transformer switcher as well as providing the needed drive capability to the FET switches.

Use of FETs as analog switch, FET current ratings, transformer and its principles of operation were also discussed, concluding with a discourse on surge suppression and its techniques.

CHAPTER THREE

SYSTEM IMPLEMENTATION

3.1 CIRCUIT APPROACH

The developed UPS in this project is divided into six major blocks as shows below in figure 3:1

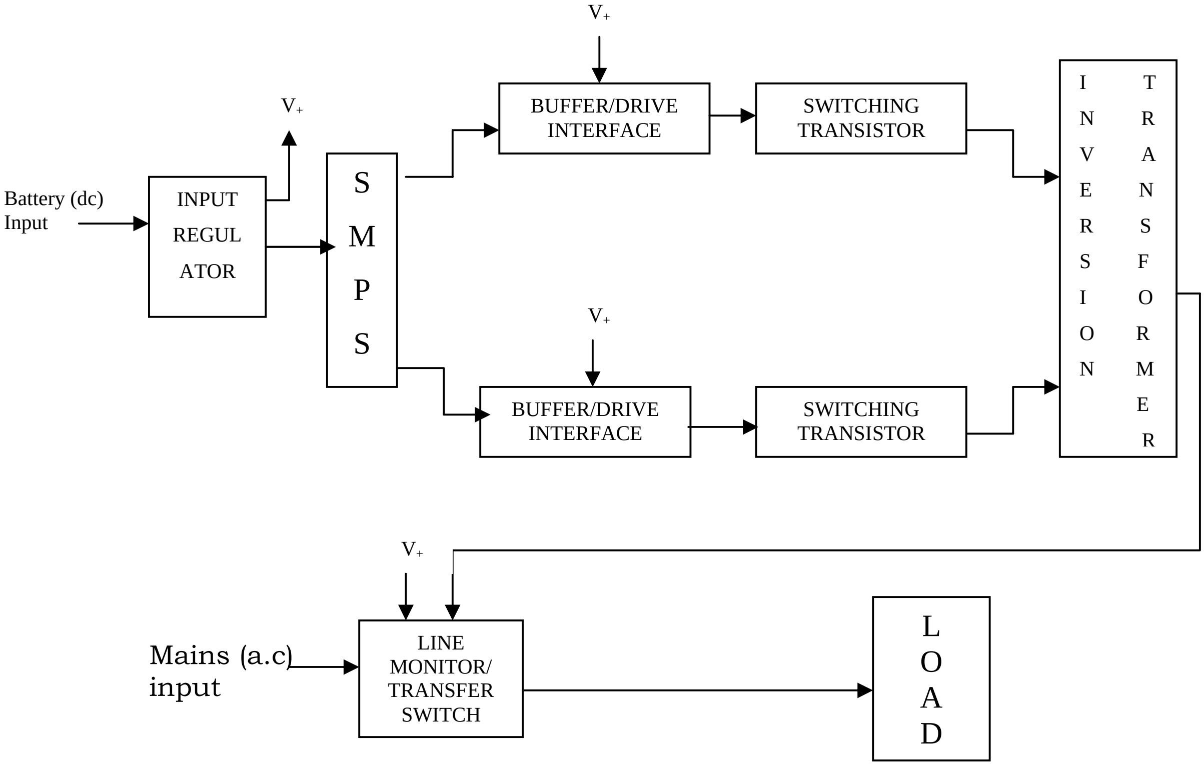


Figure 3:1 Block representation of the line-interactive UPS.

The dc power input from the battery is regulated by the input regulator. The regulated output serves as power source to the rest of the circuit.

The heart of the circuit is the dedicated pulse width modulator IC unit which provides many desired control features such as frequency setting, soft starting, overload protection, pulse width modulation and variable dead time facility. The two outputs from this SMPS are fed to the two blocks of buffer/drive interface, one each.

This interface stage acts to further ensure frequency stability (may drift due to load variation) and to provide adequate ‘hard’ drive level to the switching transistors.

The switching transistor function essentially as a push-pull amplifier that are alternatively turned or driven full ON and then OFF to impress a rectangular wave form across the primary of the center tapped inversion transformer. The transformer steps up the impressed voltage and passes it to the load via the transfer switch/line monitor block.

The line monitor/transfer switch block determines which of the two inputs sources (mains or inverter output) is to be connected to the load.

3.2 VOLTAGE REGULATOR STAGE

The voltage regulator is built around a three-terminal type fixed-voltage regulator IC, LM 7812. The circuitry is configured as shown below in Figure 3.2. The IC input ranges from +14.8V to 34V and can provide an output current of up to 1A and a power output of up to 15W.

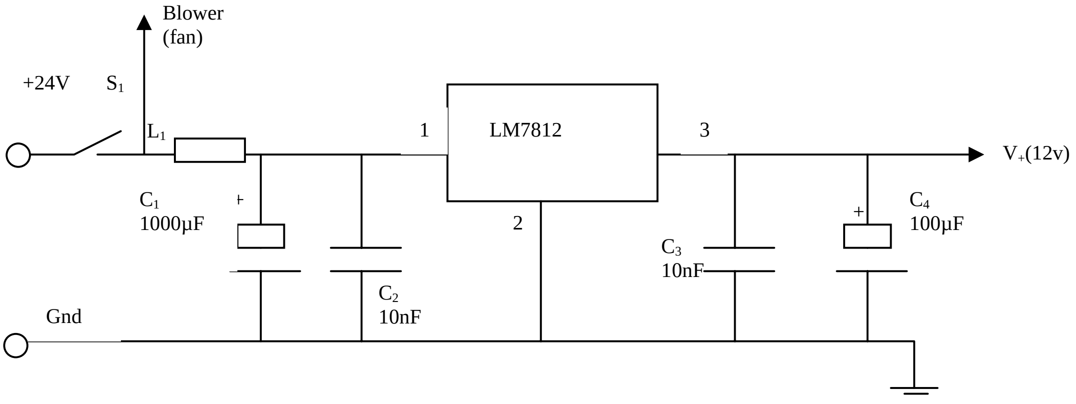


Figure 3:2 Regulated power supply for the circuit.

The switch S_1 turns the fan (not shown) ON as well as supplying the rest of the circuit through the regulator. The inductor/choke, L_1 prevents supply noise generated by the fan from upsetting the LM7812 regulator, IC. Capacitors C_1 and C_2 provide low and high frequency decoupling C_3 and C_4 provide the same function at the regulator output as well as aiding supply stability. It was observed that the IC1 generated heat when in use. As a result, it was mounted on an appropriate heat sink for a faster heat dissipation. The provision of heat dissipator aids stable operation of the IC, as well prolonging its life span. Refer to the main circuit diagram in the subsequent subsections that follow.

3.3 THE PULSE-WIDTH MODULATOR

This being the heart of the circuit, the SMPS (SG 3524) holds the ace in the overall operational control functions on the side of the inverter. Refer to the main circuit diagram.

The frequency of operation is determined by the external R-C components and it is half the oscillator frequency of the IC. The oscillator frequency is given by:

$$F_{osc} = \frac{1.43}{RC} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 3.1$$

Where R is the resistance in ohms connected from Pin6 to ground and C is the value of the capacitor connected from the IC’s Pin7 to ground respectively.

With the operational frequency specified to be 50HZ, it therefore implies that the oscillator frequency has to be 100HZ.

Choosing the capacitor value to be 10 nanofarads, i.e. 0.1μF, the resistance value is thus determined as follows from equation 3:1

$$F_{osc} = \frac{1.43}{RC}$$

$$R = \frac{1.43}{F_{osc}.C}$$

Substituting values, we have

$$R = \frac{1.43}{100 \ x\, 0.1\, x\, 10^{-6}}$$

$$= \frac{1.43}{10 \ x\, 10^{-6}}$$

$$= 143 \ x\, 10^{3} = 143 \ K\Omega$$

A fixed 120KΩ resistor is connected in series with a variable 47KΩ resistor from which the 143KΩ resistance value can be obtained. This method was adopted to counter the effect of resistor tolerance on the frequency were only a fixed value resistor used.

With pin 8 of the IC effectively on the ground potential, the supply terminal, pin 15 was wisely taken to the supply regulator output (V+) and not the entire circuit supply rail (V_{cc}). The wisdom (gotten from experimentation) behind this is to allow the unit to be already running before the drive stage gets supplied. This is to ensure its stable operation. The leading time is adjustable by the timing circuit that controls the drive supply relay, RLY1. Though the circuit will work with out this provision except for the initial circuit loading effect that is being envisaged. Resistors R_3 and R_5 attenuates the reference voltage to a desired level (5V) and feeds the rest of the circuit where it is required.

The overload limit setting is provided by the variable resistor VR_2 via capacitor C_7 to the compensation terminal Pin 9. With an overload condition in place, the IC shunts off itself. Repeated attempts to resume normal operation at a rate determined by charging and discharging of the capacitor C_7 will be defeated unless the overload is removed.

The output voltage control and hence the duty cycle is accomplished through the feed back loop from the inverter output through transformer T_2 and diode D_5 to the inverting terminal pin 1. The output of T_2 is filtered by C_5 and attenuated by a voltage divider network comprising of R_1, VR_1 and R_2. It is evident that the VR_1 sets the inverter output voltage level. The feedback signal is compared with the internal reference voltage and hence negative or positive adjustment takes place to set duty cycle level.

Diode D_7, resistor R_6 and capacitor C_8 combines to safeguard the integrity of the overload information to the compensation terminal.

The IC outputs are taken from pins 12 and 13 being collectors A and B respectively. These are used as inputs to the next stage -the interface.

3.4 THE BUFFER/DRIVE INTERFACE

The buffer/drive current boost interface is built around a complementary symmetry class – B push-pull amplifier and BIpolar – MOSFET (BI-MOS) switch. A pair of closely-matched but oppositely doped transistor T_1(C1383-NPN) and T_2(A683 – PNP) and same arrangement for T_3 and T_4 respectively form the symmetrical class-B Push-pull for each drive line, while transistor T_7(T1P42-BIpolar) and T_5 (1RFZ44–MOSFET), and similar arrangement with T_8 and T_6 respectively make up the BI-MOS switch on each drive line. Recalling the operation of the push-pull and the BI-MOS switch as treated in sections 2.7.1 and 2.7.2 respectively, this interface provides no phase inversion, has high input and low output impedances and is capable of providing fast current sourcing and sinking for the next stage - the switching transistors.

3.5 THE MOSFET SWITCHING STAGE

This stage receives gate signal from the previous stage. It is, following the signal path from the SMPS, comprised of four MOSFETS on each array, that alternately switches full ON or OFF to drive the inversion transformer. One bank is comprised of transistors T_9 – T_{12} (IRF540) while the other bank is comprised of transistor T_{13} – T_{16} (IRF540). Each of there MOSFETS has a protective input gate resistor of value 150Ω and a pull-down resistor of value 10KΩ. The importance of the series gate and the pull-down resistors have been appropriately treated in section 2.8 and their value selection have also been appropriately referenced therein.

From the specification:

Input voltage, V_{in} = 24V

Expected output power = 1500VA = P_{out}

Assume input power, P_{in} = output power, P_{out} = 1500VA.

With each MOSFET rated at maximum current, I_{Dmax}, of 28A, we can calculate the number of MOSFETs needed in each bank as follows;

Let the number of needed FETS = N

We know that power (P) is equal to the product of current (I) and the voltage (V), that is;

P = IV

$P_{IN} = I_{Dmax} X N X V_{in}$, where I_{Dmax} and V_{in} are as defined earlier.

Thus,

$$1500 = 28 \; xNx \; 24$$

$$\therefore N = \frac{1500}{672} = 2.23 \; FETS$$

Rounding off, we have 3 MOSFETS.

As it is not safe to drive the FETs at maximum current, four (4) numbers were used in each bank. This will translate to a current of about 15.625A in each of them, just a little above, half their rated current capacity.

Running the system with a power factor (P.f) of 0.9 would translate to a true power of:

$P_{True} = P_{VA} X P.f$

$= 1500 X 0.9$

$= 1350$ watts

output fuse rating at 240 volts

$$I_{fuse} = \frac{P_{True}}{220}$$

$$= \frac{1350}{240} = 5.625\ Amp$$

It is therefore safe for the system to feed load through a fuse of current rating of 5.625Amps or less. I used a 5.5A fuse. Adequate heat sink was provided in addition to a blower for fast heat dissipation. Two paralleled 0.47Ω/10w resistors were also connected from the source of each FET to ground for equal current sharing. These resistors can be eliminated with proper circuit lay out as paralleled FETS traditionally don't require current equalizing resistors.

3.6 THE SUNBBER NETWORK

The high voltage output waveform can exhibit a nasty voltage transient, with the potential to mess up the output voltage across the connected load and possibly destroy the inverter MOSFETS. As a result, a snubbler (or zobal) network comprising of two diodes (D_{10} and D_{11}), two series 100 Ω resistors (R_{47} and R_{48}) in parallel with a 220μF/200V electrolytic capacitor, C_{10}, was incorporated to slow the right time at switch on of each FET bank, reduce radiated harmonic and soften the decay of magnetic field. All these effects culminate in a gross reduction or near elimination of the adverse effect of magnetic kick-bank from the inversion transformer on the FETS.

It is to be noted that “ac” snubbers allow their capacitors to completely charge and discharge each cycle of the switching waveform and at higher frequencies will dissipate a lot of power.

It is to be remembered too that the energy required to charge a capacitor to a certain voltage and discharge it to its original level is the product of the capacitance and the voltage attained across the capacitor during the charging cycle. The snubber power, ($P_{snubber}$) dissipation is therefore:

$P_{snubber}=V^2_{(supply)}xC_{(snubber)}xf_{(pwm)}$, where $f_{(pwm)}$ is equal to 50Hz

$= 24^2 \times 220 \times 10^{-6} \times 50$

$= 576 \times 11 \times 10^{-3}$

$= 6.336$ watts

This power is dissipated through the two series 100/ 10 watts choke resistors R_{47} and R_{48} respectively. The peak reverse voltage of the two diodes, D_{10} and D_{11} used to protect the FETs against excessive current during switching interval must be more than twice the supply voltage. The IN5408 diodes that were used have a peak reverse voltage of 1000V and forward current of 0.9A.

3.7 THE INVERSION TRANSFORMER AND ITS PARAMETERS

The last stage of the developed UPS is the inversion transformer. This is a step-up transformer that converts the impressed rectangular voltage on its primary to an a.c voltage at the secondary side. The transformer has a center tapped primary side and a multiple taps secondary side to allow flexibility in its utilization.

The transformer efficiency = 90% (typical)

Primary voltage V_p = 24V

Secondary voltage V_s = 240V

Number of turns in the primary coil = N_p

Number of turns in the secondary coil = N_s

$$I_{fuse} = \frac{P_{True}}{220}$$

$$= \frac{1350}{240} = 5.625 \ Amp$$

:. Turn ratio, n $= \frac{Np}{Ns} = \frac{Vp}{Vs} = \frac{24}{240} = \frac{1}{10}$

Hence the turn ratio is 1:10

In the classical transformer equation, the muter of turn is as from equation 2.6 given by

$$N = \frac{V}{4.44 \ \Phi_m \ f}$$

It is true that we can specify the voltage, the frequency, but for a core made up of silicon-steel laminations, how does one specify the saturating flux density, Φm. The fact that the onset of magnetic saturation is relatively gradual in silicon steel, flux density is nebulous and undefined. There are other unknown parameters when this approach is used. For example, it is difficult to estimate the hysterisis and eddy-current losses in such cores.

These losses, which have a significant effect in the operating efficiency at frequencies greater than 400HZ, also have often adverse effects.

It is known that optimization of transformer efficiency occurs when the core and copper losses are equal. How to bring about this condition without extensive data acquisition and computer–aided design has been a problem beyond the capabilities of most workers in the field.

The above problem led to the adoption of the volt per turn principle in the transformer winding. The volt/turn (v/t) is the voltage a single turn of copper wire can carry or hold in a given magnetic field.

Bearing in mind the amount of current in the primary windings (62.5A) and the secondary windings (6.25A), suitable wire size was selected for the two windings as gauge 10 and gauge $17^1/_2$ respectively, as they are popularly graded and called.

I started the winding with the secondary side. Experimenting with the use of variable ac source (via a variac), I arrived at a volt /turn of 0.9V with 150turns on the former (core) and a voltage of 135V supply connected across, I had a current of 0.4A in an ammeter connected in series with the line. It was comfortable for me at this level as I intend to have a no –load current of 0.5A to prolong the copper wire insulation and that of the transformer ultimately.

Therefore, with my selected output voltage of 240v, the number of turns on the secondary winding is calculated thus:

$$Ns = \frac{Vs}{{}^{v}/_{t}} = \frac{240}{0.9} = 266.6667 = 267 \ turns$$

$$Hence Np = Nsxn \ (turnratio)$$

$$= Nsx \ \frac{1}{10}$$

$$= \frac{267}{10} = 26.7 = 27 \ turns$$

The 27 turns on the primary would translate to a 24.3V on the primary side winding with the 240V on the secondary side winding.

3.8 THE LINE MONITOR/TRANSFER SWITCH

This stage is built around comparators A1, A2, A3 and a 555-time IC. to act as a “window comparator” used to set the ‘low’ and ‘high’ input ac. voltage acceptable limits. The transformer T_3 is used to sense the presence or absence of the public mains supply. Actually, the T_3 is made of two (220v-12v_{ac}) step-down transformers in series.

The wisdom behind this arrangement is to supply the primaries of these transformers at half their related voltage so that input voltages of even up to 440V_{ac} will not cause them any problem.

The secondaries of these are rectified and serve as input to the window comparators.

Comparators A_1 and A_2 set the lower acceptable limit (210Vac), in this case, via the variable resistor RV_4. The operation is such that if the non-inventing terminal of A_1 sees a voltage lower than the reference (+5v) voltage, its output swings to near V_{cc} value (12v) via the ‘pull-up’ resistor R_{48}. The output of the A1 is connected to the inventing terminal of the second comparator A_2. The comparator A_2 compares this value (almost V_{cc}) with the reference voltage on its non-inventing terminal with the resulting low output voltage value (near ground) that is connected to pin 2 of 555-timer IC, which is configured as a monostable. With a `low` at the pin 2 of this monostable, the output (pin 3) goes high to bias the transistor T_{17} on and hence energizing the main relay, RLY_1, to make for inversion process.

Another condition that will make the output of this monostable high again is a no-mains situation.

This would mean a no-signal at pin 2 of the 555-timer monostable implying a 'high' output that would equally bias ON the T_{17} to energize RLY_1.

The ideal of using the monostable at the output of this low voltage level limiter is to avoid the unwanted vibration/ oscillation which I experienced during the project development when supply fluctuations kept manifesting in multiple change over. With the resistor R_{50} (100KΩ) and the capacitor C_{14} (47μF), I had a 5.17 second ($t=1.1RC$) breathing space, offered by the monostable circuit, should the supply suddenly fall bellow the set level and normalizes almost immediately, before the system goes back to supply the load from the mains again

The 'high' ac input level (250Vac) is set by the comparator A_3 via the variable resistor RV_5. The operation of this comparator is such that when a higher-than–reference voltage value is sensed at its non-inverting terminal, its output level goes high (almost V_{cc}) and this goes to bias the energizing transistor T_{17} for the main relay, RLY_1, to make. So long as the ac input voltage is above 250 Vac, the A_3 output remains high and a measure of stability (hysterisis) is provided it (output) via the 100kΩ resistor, R_{52}, and the capacitor, C_{12}.

Similar arrangement of the monostable out put would have being made for the high voltage level side too out but for limited resources.

It is to be noted that the main relay, RLY_1 has three contactors labeled RLY_{I1}, RLY_{I2}, and RL_{I3} as show on the circuit diagram sheet 4.

Relays RLY_2 and RLY_3 respectively control the drive, stage power supply (V_{cc}) and charging order command during “normal” mains supply to the connected load.

A full-charge-disconnect relay (RLY_4) and its drive circuitry is incorporated to stop the battery from receiving charging current should the battery be fully charged during normal mains supply, as sensed by battery voltage sensor. The sensor forms part of the drive circuitry for the RLY_4.

3.9 OVERALL CIRCUIT DIAGRAM

The complete circuit diagram of the developed 1500VA line-interactive UPS is shown in figure 3.3(a)-(d). It shows clearly all the interconnections between the various components and subsystems that make up the UPS presented in this thesis.

3.10 CONSTRUCTION AND ASSEMBLY

The construction of the 1500VA UPS is divided into five sections:

i) Input terminals
ii) Output socket terminal (outlet)
iii) Printed circuit board
iv) Heat sinks
v) Transformer

The input terminals consist of two thick (35mm) cables marked positive (+) and negative (-) which link the dc voltage supply to the circuit board and the center tap of the inversion transformer. The negative (-) cable is solidly soldered and bolted to the body of the UPS unit to reduce voltage drop as well as reduce heating through the heavy current return path.

The ac input cable consists of a twin flex marked “AC IN” and is connected to the transfer switch.

All these cables are passed into the UPS cabinet from the rear.

The output socket (outlet) is mounted at the rear also with proper wiring connections made to the secondary welding of the inversion transformer through the transfer switch. The output fuse, F, was also mounted at the rear.

The printed circuit board provides all the circuit components with mounting bases while its tracks provide interconnection paths. Cable links were used from one board to the other. The cables were kept as short as possible.

All components were fitted into the layout on the printed circuit board (PCB) and soldered, starting with resistors, through diodes, IC sockets, capacitors, and the transistors in that order ensuring correct polarity after they had been tested and confirmed alright using digital multimeter. The ICs were then plugged in lastly and test again.

The eight power MOSFETs were tested for reliability and firmly mounted on to two separate heat sinks with four (4) MOSFETs being paralleled on each. The heat sinks are in direct contact with the drain terminals of the FETs. Thick cable (25mm) was used to connect each of the heat sinks to each side of the transformer primary windings, after it (transformer) had been firmly mounted on to the base of the UPS 'casing' using bolts and nuts. The center tap of the transformer was connected to the positive terminal of the 24Vac battery source.

Two power switches, one each at the front and rear, are mounted to give control on the use of the UPS unit. The front power switch is a push-to-ON switch that switches power to the control circuit while the rear switch is used to switch on the mains supply.

Two 'LEDs', used to indicate when UPS is in use (red) and when the mains is in use (green), are mounted on the front cover to give visual indication of the UPS status.

With all components now on board, all the circuit modules mounted and their interconnection paths made, the entire circuit was checked and tested for continuity with the aid of a digital multimeter.

3.11 TESTING/RESULTS

Test was carried out on each of the modules as being constructed, and the entire circuits as a complete system.

The output voltage of each stage was measured with a digital multimeter and the final output was monitored on the oscilloscope

The results obtained are as follows:-

i) A voltage of 2.4Vdc was measured at the output pins (Pin 12 and Pin 13) of the pulse width modulator IC. The frequency measured was 50Hz. Figure 3.4 below is an illustration of the quasi-sine waveform as seen on the oscilloscope from the IC's out pins.

ii) A voltage reading of 6.5Vdc was obtained at the outputs of the buffer at test points U_1 and U_2 respectively. The frequency and waveform at this stage is the same as that obtained from the previous stage.

iii) A voltage of 240v was measured at the selected tap of the transformer secondary winding. The output waveform seen on the oscilloscope was a magnified replica of the "quasi" sinewaveform obtained from the pulse width modulator outputs with some frequency of 50Hz. This is shown in figure 3.5.

The stepped approximations to sinewave output obtained is most desirable as it makes it possible to meet both RMS and peak voltage requirement of different loads connected to it.

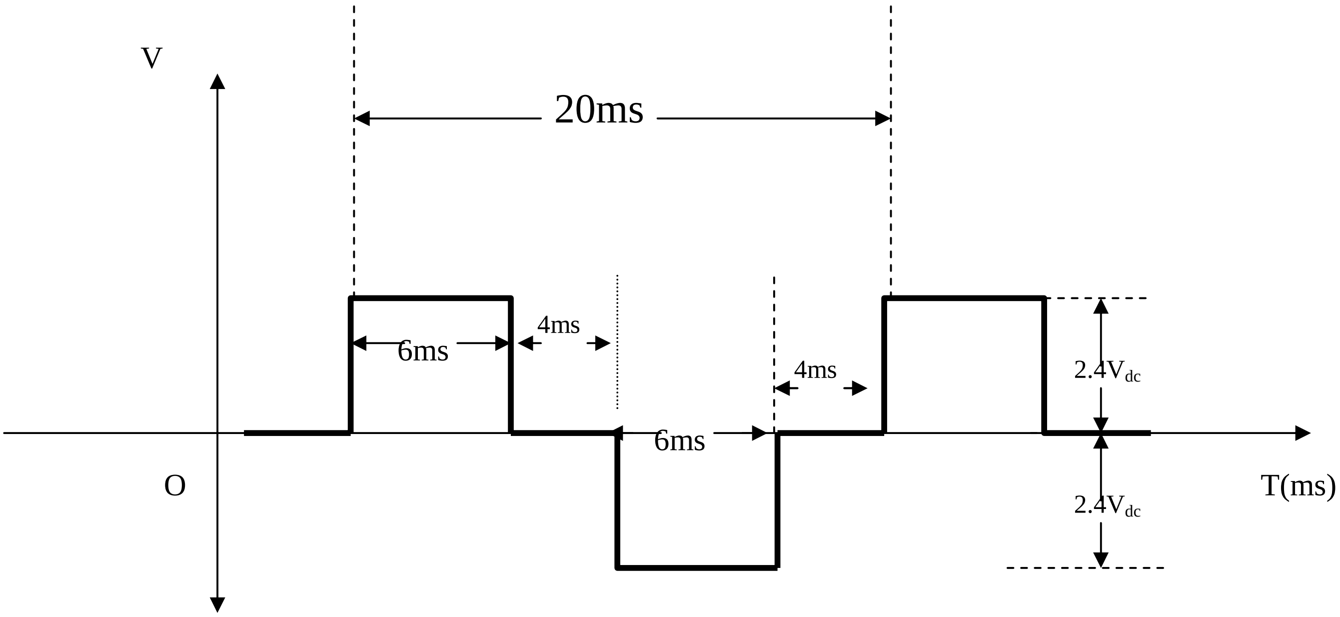


Fig. 3.4 Output wave form of the pulse width modulator

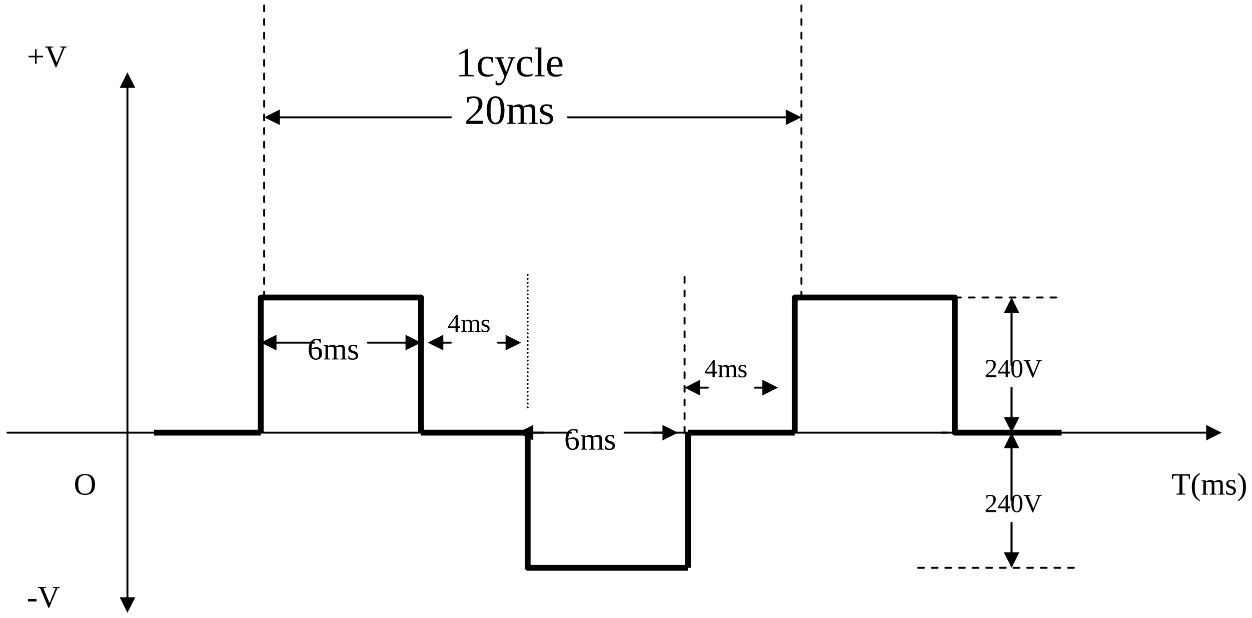


Figure 3.5 Final output voltage wave form

The transformer output voltage was also measured from all the different tappings neutral to the termal.

The measured values are as tabulated below in Table 3.1 against their corresponding number of turns using the volt/turn value of 0.9 as designed.

Table 3.1

Transformer output voltage against corresponding number of turns

S/N	Number of turns (t)	Output voltage (V)
1	150	135
2	200	180
3	211	190
4	237	213
5	256	230
6	267	240
7	289	260
8	295	265

A graphical sketch (not to scale) of the number of turn and the corresponding voltage shows a linear relationship.

This is as depicted below in Fig. 3.6

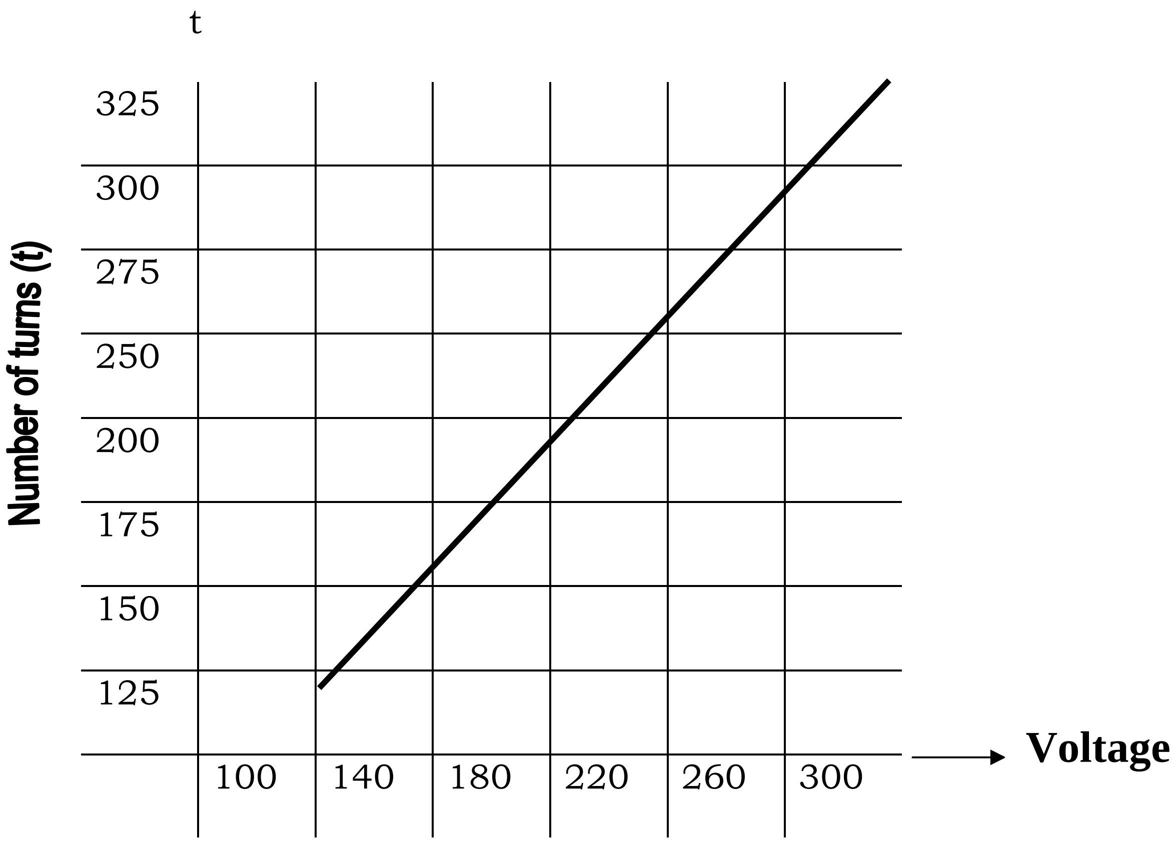


Fig. 3.6 Graphical sketch of volt/turn relationship

It can be vividly read from the graph that as the number of turns increase, there is a corresponding linear increase in the voltage output measured. This shows the proportional relationship between the e.m.f and the number turns for a given transformer as contained in equation 2.6.

It is of interest too to put in record the battery terminal voltage, readings taken at selected applied load values. This is given in table 3.2 below

Table 3.2 Battery terminal voltage at selected load values

S/NO	APPLIED LOAD (W)	BATERY VOLTAGE (V)
1	0	24
2	100	23.9
3	200	23.8
4	500	23.6
5	900	23.4
6	1000	23.2
7	1200	23.0

From the above table, it is clear that the battery voltage decreases with increasing applied load, implying an inverse relationship.

The unit was then functionally tested to supply up to 1,250 Watts power for upward of 1hour without any malfunction, since Power = IV

1250watts = 24 x I

This implies a current I of 1250/24 = $\underline{52A}$

$$\text{Hence } \frac{60Ah}{52A} = \underline{1.153hrs}$$

$$= \underline{1hr\ 9mins\ 18\ secs}$$

The autonomy of the UPS can be extended by increasing the input power (battery) capacity or by reducing the quantity of connected load to less than UPS rated capacity. The final output voltage remains constant at set value (220Vac) on full load. Though you may notice a little drop in voltage as load is being connected, it does immediately stabilizes. This is solely due to the action of duty-cycle adjustment (pulse width modulation) being performed by the modulator IC and hence one of the reasons for its choice in this project.

With the applied load of 1250W at a power factor of 0.9, the UPS efficiency is calculated thus:

$$\text{Efficiency} = \frac{\text{Output (W)}}{\text{Input (W)}}$$

$$= \frac{1250}{1350} x100 = 92.5\%$$

This value shows how effective the constructed UPS is. This also means a power loss of 7.5% attributable to losses in the transformer and the power transistors in the form of heat.

3.12 PROJECT MONETARY COSTING

Presented below is a detailed monetary costing of the constructed UPS unit with the sole intent of providing a basis for cost comparison with available commercial units of equal performance ratings.

Bill of engineering measurements and evaluation for the construction of a 1500VA line interactive UPS system.

S/N	Item Description	Qty	Unit rate (₦)	Total cost (₦)
1	Inversion transformer (main)	1	11500	11500
2	Step-down transformer (12v-0-12v)	3	150	450
3	IC-SG 3524	1	500	500
4	IC-LM 393	2	50	100
5	IC-555-Timer	1	50	50
6	MOSFET (IRF 540)	8	150	1200
7	MOSFET (IRFZ 44)	2	100	200
8	Bipolar transistor – C1383	3	40	120
9	Bipolar transistor –A683	2	40	80
10	Bipolar transistor – A733	2	20	40
11	Bipolar transistor – TIP42	2	60	120
12	Capacitor-1000μF/35v	1	40	40
13	Capacitor- 100μF/25v	2	40	80
14	Capacitor-220μF/200v	1	150	150
15	Capacitor- 47μF/35v	6	30	180
16	Capacitor- 4.7μF/35v	2	30	60
17	Capacitor- 1μF/35	1	30	30
18	Non-electrolytic capacitor-10nF	2	10	20
19	Non-electrolytic capacitor-100Nf	1	10	10
20	Resistor – 0.47Ω/10W	16	20	320

21	Resistor – 1Ω/10W	1	20	20
22	Resistor – 100Ω/10W	2	20	40
23	Resistor – 18Ω/$^{1}/_{4}$W	5	5	25
24	Resistor – 150Ω/$^{1}/_{4}$W	8	5	40
25	Resistor – 1kΩ/$^{1}/_{4}$W	5	5	25
26	Resistor – 4.7kΩ/$^{1}/_{4}$W	2	5	10
27	Resistor – 10kΩ/$^{1}/_{4}$W	11	5	55
28	Resistor – 20kΩ/$^{1}/_{4}$W	3	5	15
29	Resistor – 47kΩ/$^{1}/_{4}$W	1	5	5
30	Resistor – 100kΩ/$^{1}/_{4}$W	4	5	20
31	Resistor – 12kΩ/$^{1}/_{4}$W	1	5	5
32	Potantiometer – 20k	4	30	120
33	Potantiometer – 47k	1	30	30
34	Diodes – 1N 4007	19	10	190
35	Diodes IN 5408	2	20	40
36	Zener Diodes – IN 5231	2	20	40
37	13A socket	1	60	60
38	13A plug	1	40	40
39	Relay (24v)	1	400	400
40	Relay (12v)	3	80	240
41	Fuse + fuse holder (6A)	1	70	70
42	Switch	2	60	120
43	Light emitting diodes	2	10	20
44	Metal casing	1	1600	1600
45	Front cover	1	1500	1500
46	Battery (12V$_{dc}$/60Ah)	2	4300	8600
47	Battery terminal	4	100	400
			TOTAL	₦29680:00

The above quoted prices are a function of time and place of procurement.

CHAPTER FOUR

CONCLUSION

The main aim of the study was to investigate and analyze the various UPS topologies available and to develop a realizable UPS design capable of providing an output power of 1500VA from a 24Vdc battery source that would be cost effective, reliable, maintainable and tropicalised. A thorough investigation was firstly undertaken. A comprehensive analyses of the various identifiable UPS topologies was given in chapter two, with the line-interactive type UPS being the most attractive and preferred.

In chapter three was a detailed presentation of the design approach of the line-interactive UPS. For ease of system implementation and subsequent maintenance, the circuit was divided into two main modules.

The first module combines the input regulator, the pulse-width modulator unit and the buffer/drive interface stage with the power switching stage. On the second module was the line-monitor and the transfer switch control circuitry.

The input regulator LM 7812, used, was a three terminal, fixed voltage type. It was preferred for its unique features such as current limiting, self-protection against over temperature, foldback current limiting facilities amongst others. It has a stable output of 12Vdc.

It is desirable that a UPS should supply the protected loads with an ideal sine wave form or a stepped approximation to a sine wave form so it can simultaneously satisfy their differing peak and RMS voltage requirements without malfunction or damage. To achieve this, use was made of a specialized IC module, the SG3524, which not only provided the desired 'quasi' sinewaveform but also other control features such as adjustable dead time, overload protection, duty cycle control and hence output voltage monitoring via a feed back loop.

The buffer/drive interfare incorporated provides additional stability and fast switching speed to the circuit operation through the complementary symmetry class-B amplifier and the Bipolar Mosfet switch.

The complementary symmetry class-B amplifier built has high input impedance and low output impedance which provides for load matching while the BIPOLAR/ MOSFET switch cascode was used to achieve better switching performance by providing fast current sourcing and sinking to the gate capacitances of the transformer switching transistors.

Two banks of power MOSFETs, four numbers in each, alternately switch power through the invasion transformer which in turn provided a stable output voltage of 220Va.c even on full load.

The line monitor was built around a network of comparators and timing circuit. This sets the acceptable mains (ac) input levels at 210Vac (lower limit) and 2250Vac (upper limit) that can be connected to the protected load through the transfer switch. Otherwise, the transfer switch acts to put the load on the UPS output.

Later part of the chapter three gave details of the constructional approach taken to realize the constructed UPS. After the various modules had been built and tested, they were mounted in the casing specially made for the UPS with input/out points, external power control switched and status indicators appropriately positioned for ease of utilization.

The constructed unit was functionally tested to supply a load of 1250watts for an upward of one hour without any sign of malfunctions when powered from a 24V/battery source. The UPS autonomy can be extended by increasing the input power (battery) capacity or by running it at less rated power capacity. Performance test indicates a perfect voltage regulation as output voltage at full load was maintained at 220v set value.

Owing to the fact that the UPS design took into consideration loads running on 120Vac/60Hz supply, provision for them was made through the multiple taps transformer designed. It is hereby strongly advised that when this facility is to be used, the operating frequency MUST be changed via the variable resistor VR_3 accordingly and the output fuse rating be increased to stand the load current.

It is recommend, however that should this project be embarked upon by another student again, a monostable delay circuit be added to the high ac threshold setting to counter multiple changeovers similar to that provided on the ‘low ac’ threshold setting in the line monitor block.

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